Research in VLSI Design and CAD Laboratory (VDCL)

http://www.vdcl.cse.unt.edu

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Discover the power of ideas

Outline of the Talk

- About VDCL
- Ongoing Research
- Proposals
- Publications
- Patents
- Thesis/Dissertation
- VDCL Members

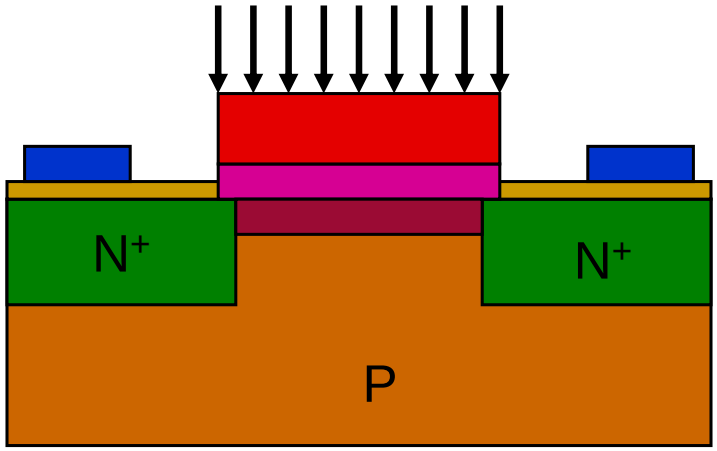
VDCL: Overview

- Established in September 2004
- Mission:
  - to carry out research in low power VLSI design
  - to prepare next generation CAD tools for automatic design
- Located at F233, Research Park.
- Has strong research infrastructure including Dual-Xeon server, Sun/Linux/Windows Workstations, and Tera Bytes of storage.
- Cadence, Synopsis, and Xilinx tools will be available.

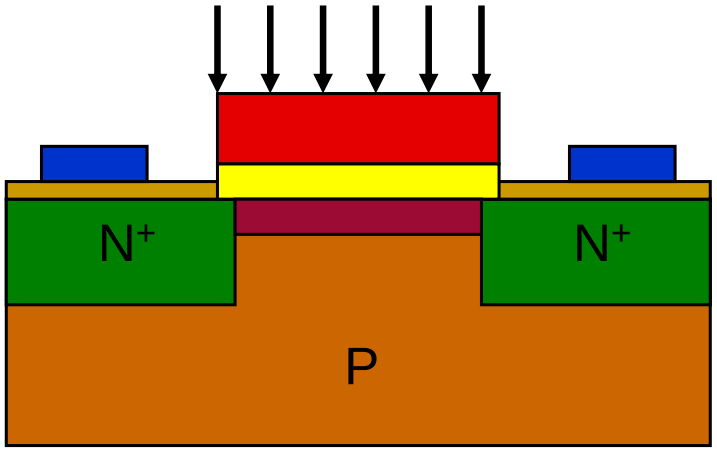
VDCL : Research Focus

- Our research is in Design and CAD for Low-Power High-Performance Nanoscale VLSI.
- This can be classified to the following *inter-related* categories:
  - Power-Performance Modeling and Optimization for Nanoscale VLSI Circuits
  - Design and CAD for Nanoscale Digital and Analog/Mixed-Signal Circuits
  - VLSI Architecture for Multimedia Processing
- We develop power, leakage, and performance models, incorporate them in CAD flow through optimization methodology, and demonstrate them through computational intensive multimedia applications.

Ongoing Research: DKCMOS

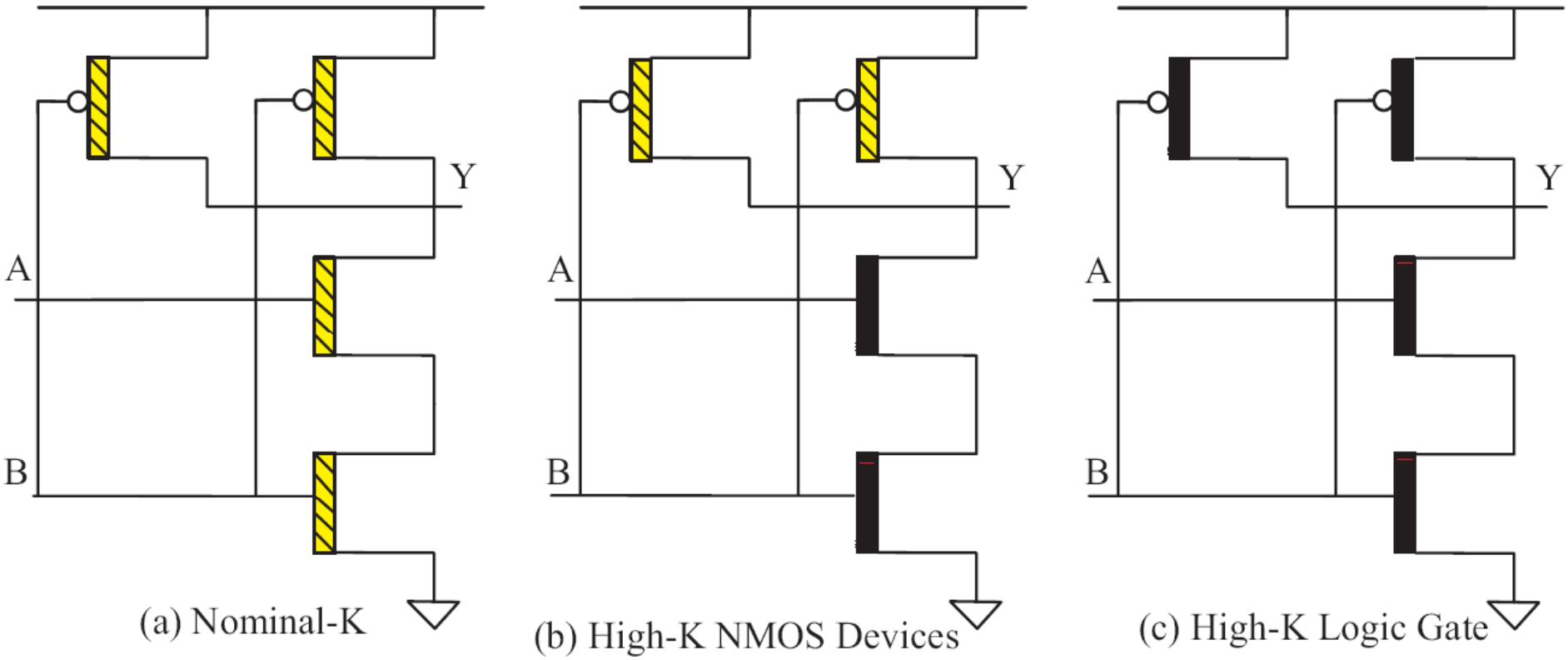


Low K_{gate} → Larger I_{gate} , Smaller delay



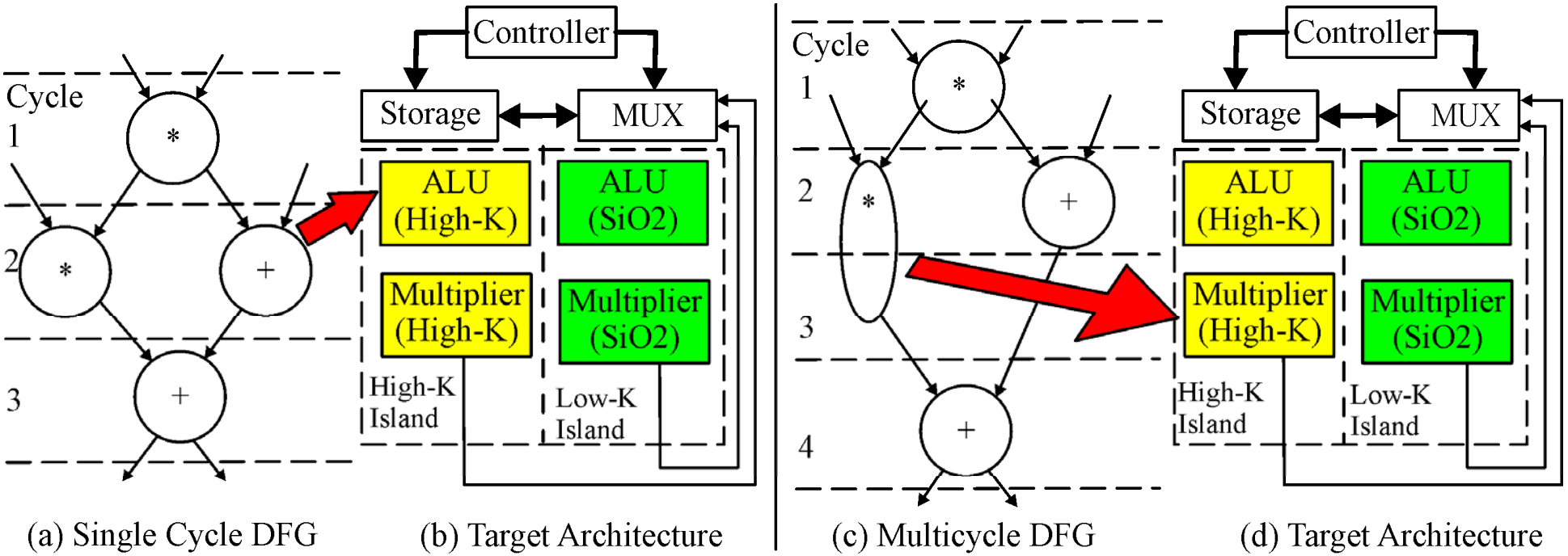
High K_{gate} → Smaller I_{gate} , Larger delay

Ongoing Research: DKCMOS



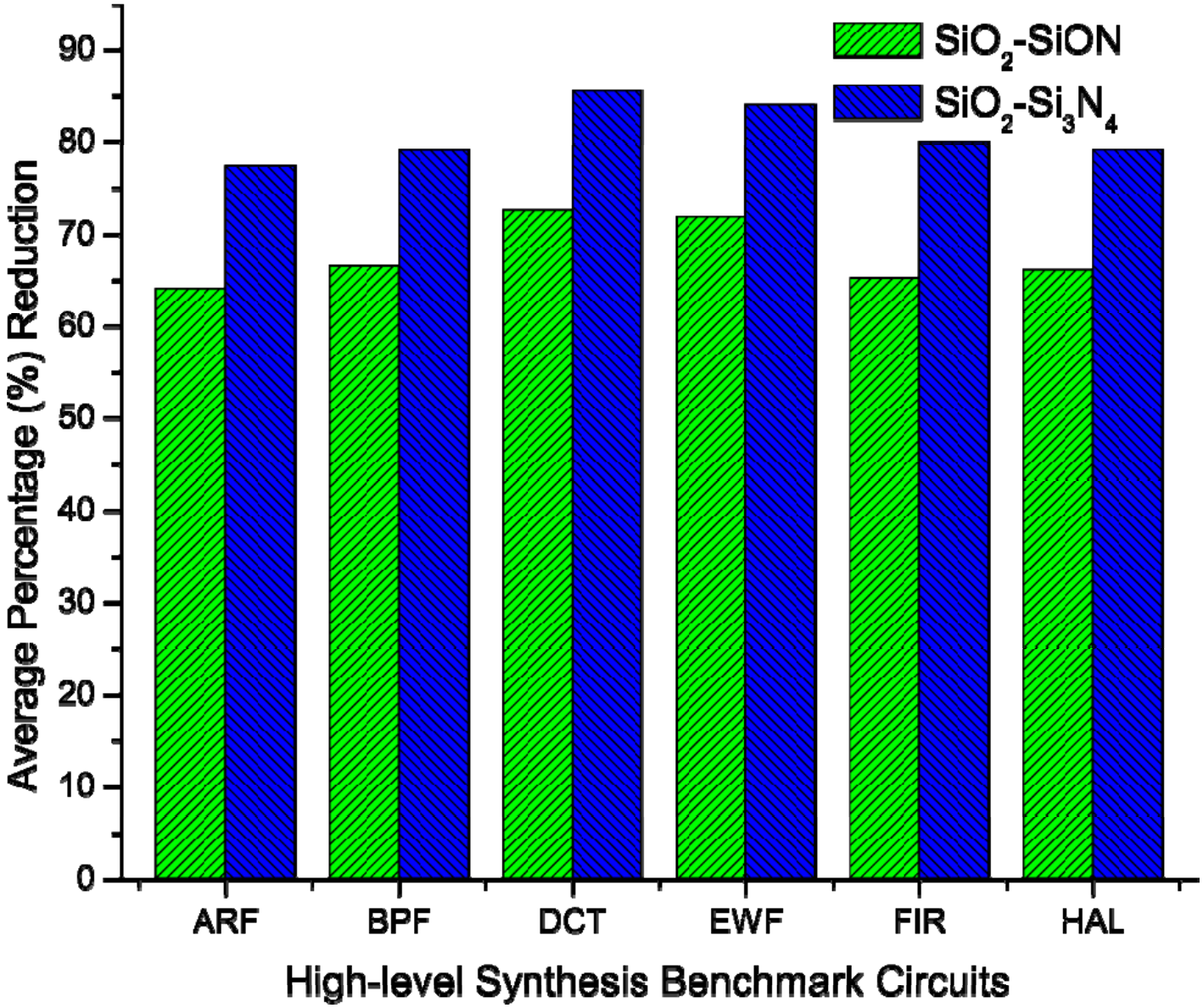
(a) Nominal-K (b) High-K NMOS Devices (c) High-K Logic Gate

Ongoing Research: DKCMOS

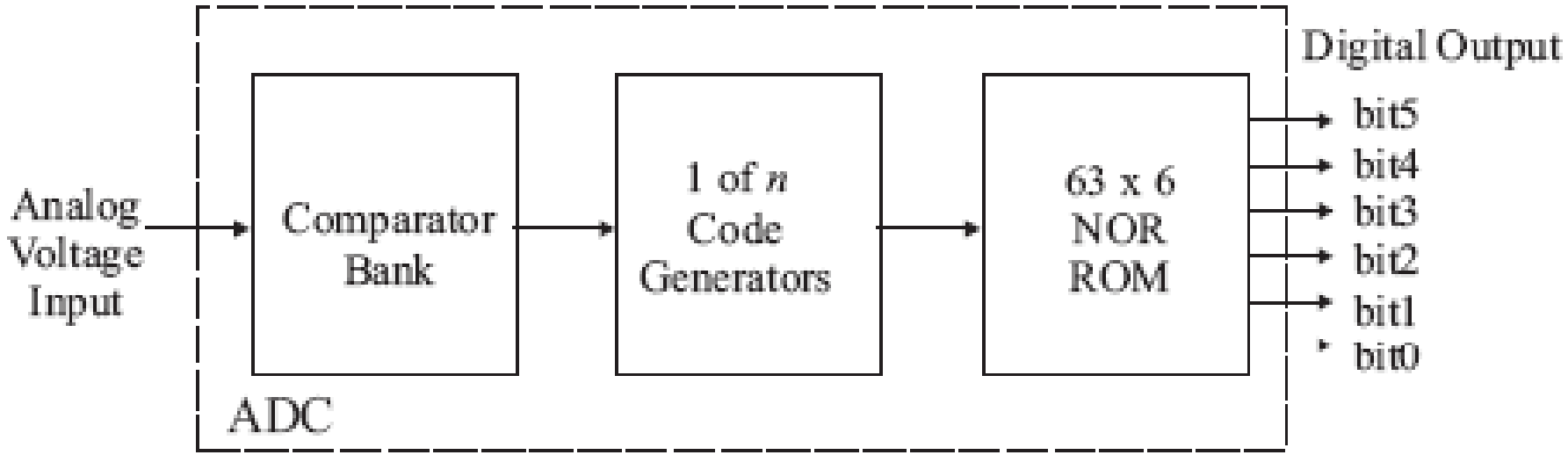


High-K and Low-K Islands

Ongoing Research: DKCMOS



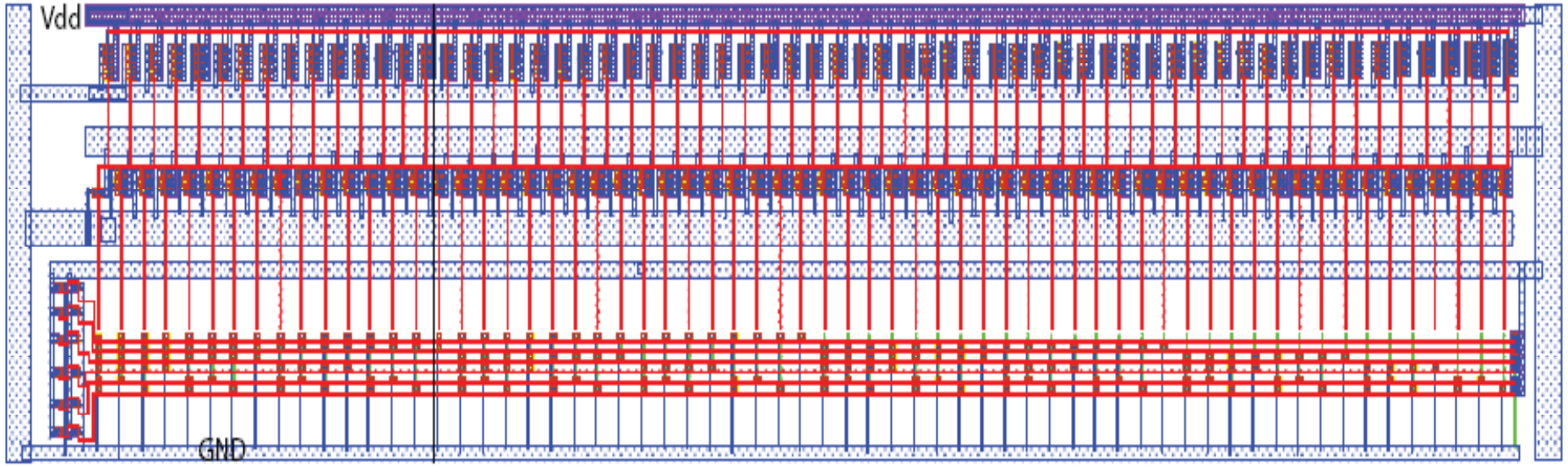
Ongoing Research: ADC



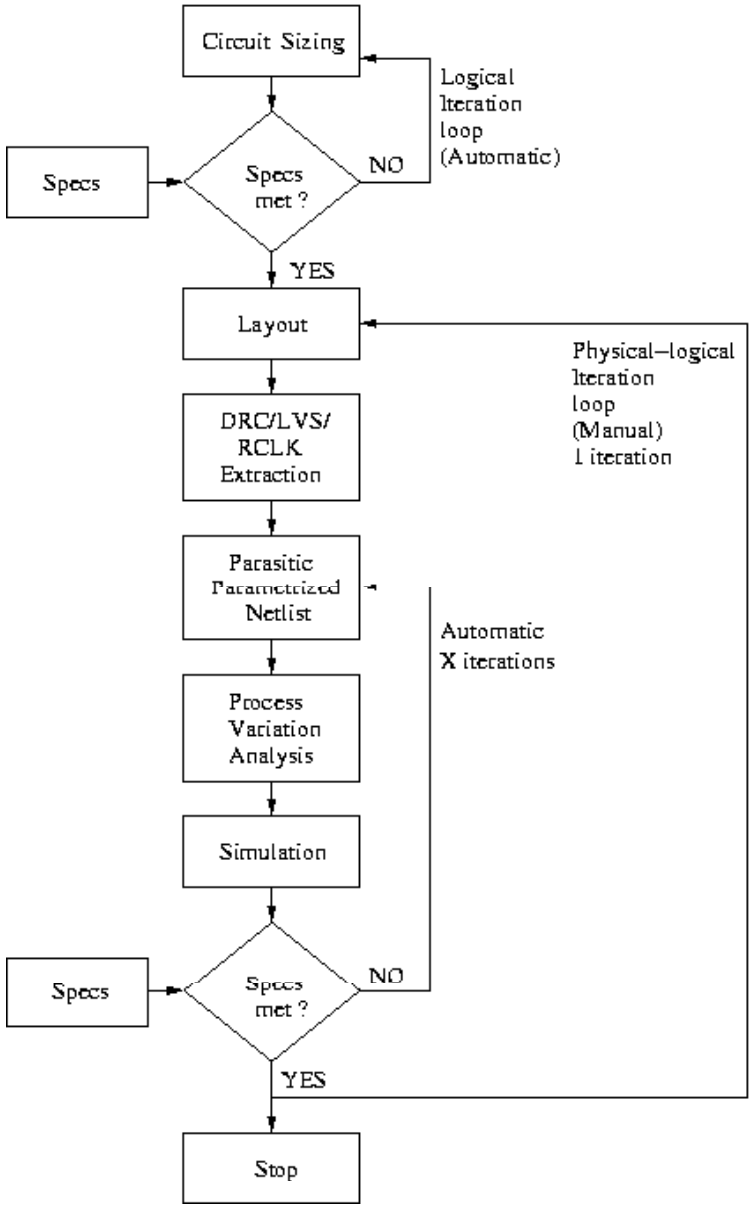
- Output of Comparator Bank is thermometer code.
- Converted to 1-of n code using 1-of n code generators.
- NOR ROM converts the 1-of n code to binary code.

Ongoing Research: ADC

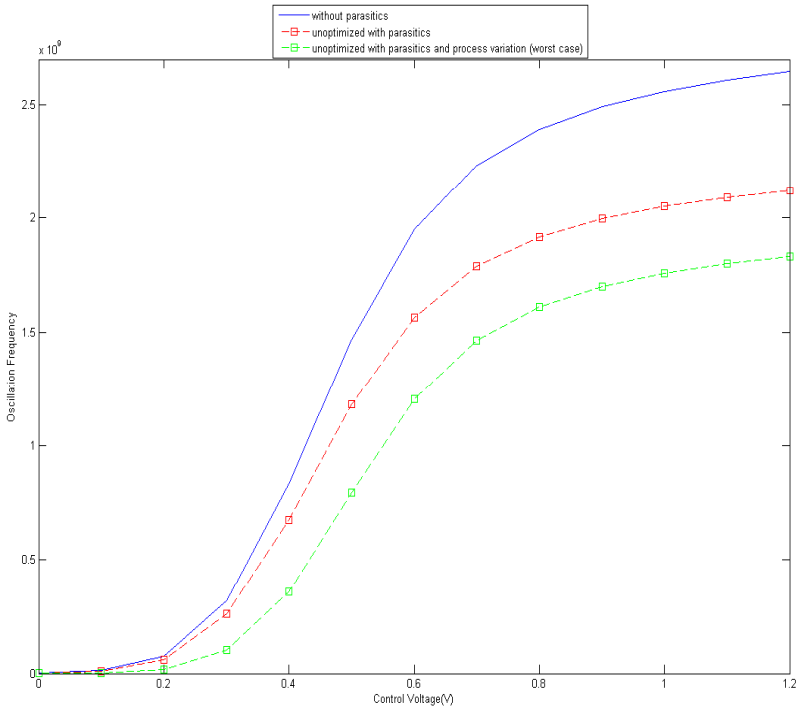
- Physical design of the ADC carried out using 90nm Salicide “1.2V/2.5V 1 Poly 9 Metal” digital CMOS pdk, demonstrating SoC readiness.
- To ensure minimal IR drop, power and ground routing comprises of wide vertical bars and generous use of contacts has been made.



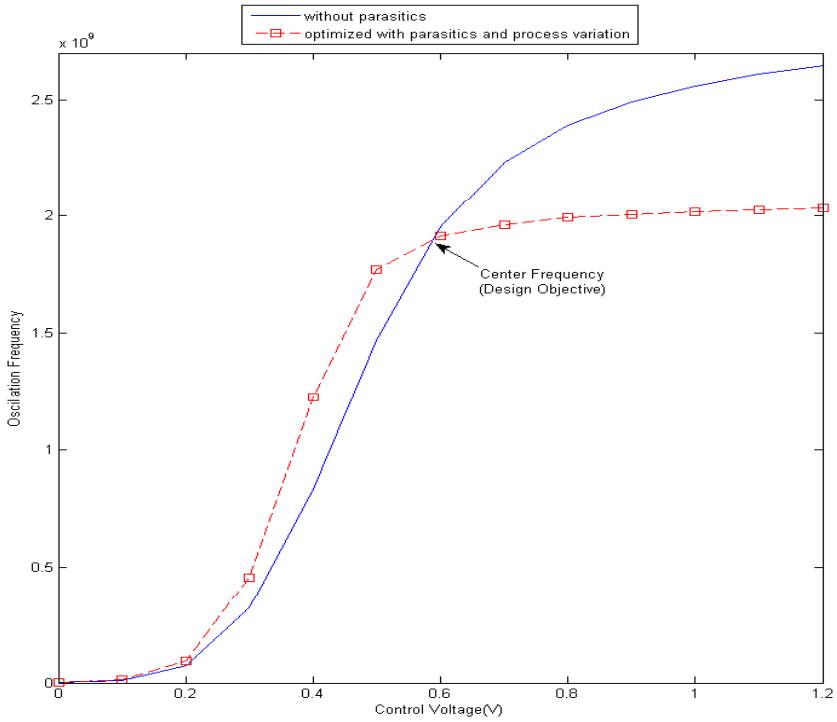
Ongoing Research: VCO



Ongoing Research: VCO



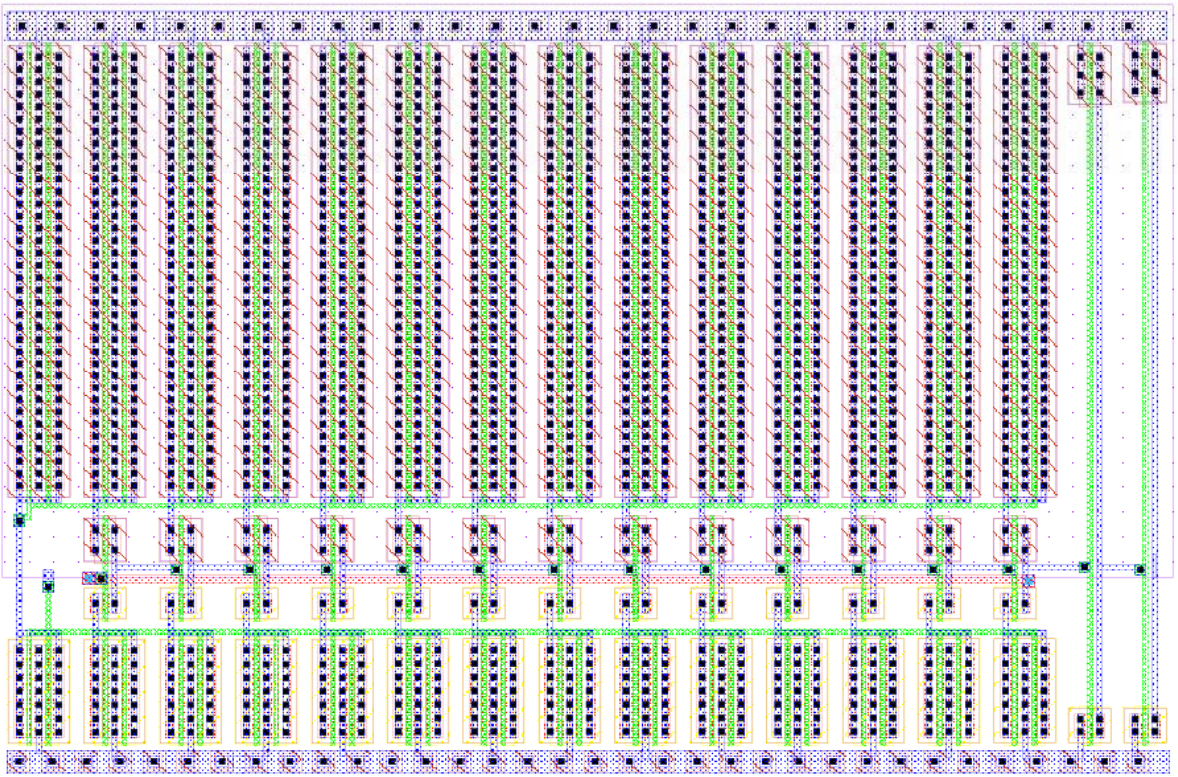
Before Optimization.



After Optimization.

Ongoing Research: VCO

- Physical design carried out using a 90nm salicide 1.2V/ 2.5V 1 Poly 9 Metal process.
- Full extraction including resistors (R), capacitors (C), inductors (L) and mutual inductors (K) is performed.



Proposals

- A Comprehensive Methodology for Early Power-Performance Estimation of Nano-CMOS Digital Systems, National Science Foundation (NSF), CCF – Computing Processes and Artifact (CPA), 2007-2010, amount - $200,000.

Publications

- **Summary**: **14 peer-reviewed top-notch journals and 51 peer-(blind)reviewed to-notch conference publications**.
- **S. P. Mohanty**, et al., “Simultaneous scheduling and binding for low gate leakage nano-complementary metal-oxide semiconductor data path circuit behavioural synthesis”, *IET Computers & Digital Techniques (CDT)*, March 2008, Volume 2, Issue 2, pp. 118-131.
- **S. P. Mohanty**, et al., “ILP Models for Simultaneous Energy and Transient Power Minimization during Behavioral Synthesis”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 11, No. 1, January 2006, pp. 186-212.
- **S. P. Mohanty**, “ILP based Gate Leakage Optimization using DKCMOS Library during RTL Synthesis”, in *Proceedings of the 9th IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 174-177, 2008.

Patents

- Methods and Devices for Enrollment and Verification of Biometric Information in Identification Documents, US Patent filed on 24th April 2008.
- Apparatus and Method for Transmitting Secure and/or Copyrighted Digital Video Broadcasting Data Over Internet Protocol Network, Provisional Patent filed on 30th November 2007, Application Number 61/004,044.

Thesis/Dissertations

- 12 thesis completed.
- 3 thesis and 2 dissertations are in progress.
- S. Tarigopula, M.S.(Computer Engineering), Thesis: “A CAM based High-Performance Classifier-Scheduler for a Video Network Processor”, Spring 2008. (**Received Outstanding Master’s student in Computer Engineering Award for year 2007-2008.**)
- G. Sarivisetti, M.S.(Computer Engineering), Thesis: “Design and Optimization of Components in a 45*nm* CMOS Phase Locked Loop”, Fall 2006. (**First UNT woman Computer Engineering graduate with VLSI specialization.**)
- V. Mukherjee, M.S.(Computer Engineering), Thesis: “A Dual Dielectric Approach for Performance Aware Reduction of Gate Leakage in Combinational Circuits”, Spring 2006 (**First UNT Computer Engineering graduate with VLSI specialization.**)

Current VDCL Members

- Saraju P. Mohanty, Director.
- Elias Kougianos, Asst. Professor, Dept of Engineering Technology.
- D. V. Ghai, Ph.D.(Computer Science and Engineering) student.
- M. R. Ratnani, Ph.D.(Computer Science and Engineering) student.
- S. Naraharisetti, M.S.(Computer Engineering) student.
- A. Mendoza, M.S.(Electrical Engineering Technology) student.
- P. More, M.S.(Electrical Engineering Technology) student.

Thank You