Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design

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Summary and Conclusions

- We present a novel parasitic and process variation aware methodology for performance optimization of radio frequency (RF) circuit components.
- The proposed methodology performs the multiple iterations automatically on a parasitic parameterized netlist derived from the layout. The manual iteration is reduced to 1.
- The degradation in the oscillation frequency of an RF VCO due to parasitic and process variations has been narrowed down from 43.5% to 4.5%.
- Future work will address simultaneous optimization of frequency, linearity response, phase noise etc.

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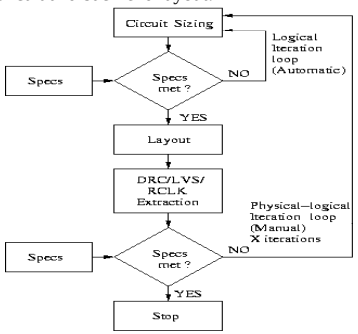
Abstract

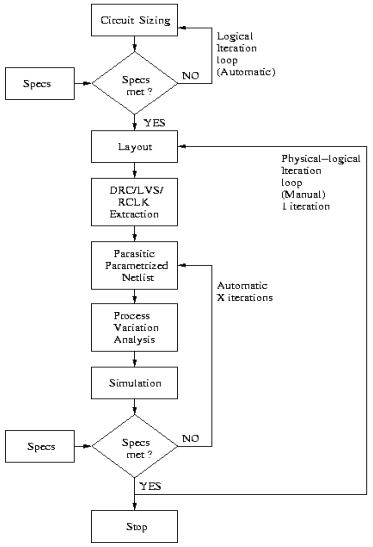
- *At nanoscale technologies, process variations have significant impact on circuit performance and need to be included in the design cycle. RLCK parasitics cause further performance degradations.*
- *We present a parasitic aware, process variation tolerant design methodology. A 90nm current starved VCO has been treated as case study.*
- *The oscillation frequency of the VCO is the objective function with area overhead as constraint. A degradation of 43.5% is observed when the RLCK parasitic extracted circuit is subjected to worst case process variation. After a **single** physical design iteration, the oscillation frequency is within 4.5% of the target.*

Introduction and Motivation

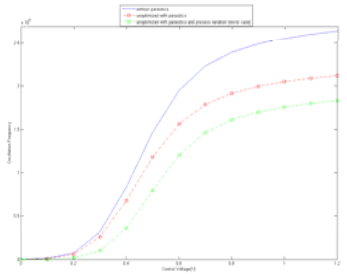
Standard RFIC design flows require multiple (X) manual iterations on the back-end layout to achieve parasitic closure between the front-end circuit and back-end layout:



The proposed methodology performs the multiple (X) iterations automatically on a parasitic parameterized netlist derived from the layout. The manual iteration is reduced to 1. To have a process variation robust design, process variation analysis is introduced in the design flow.



- Figure below shows the frequency-voltage characteristics of the VCO.
- Uppermost curve shows the characteristics for logical design. Oscillation frequency = 2GHz.
- Middle curve shows the characteristics for parasitic extracted layout. Discrepancy = 25%.
- Bottom curve shows the characteristics for parasitic extracted layout subjected to *worst case* process variation. Oscillation frequency = 1.13GHz. Discrepancy = 43.5%.



VCO Logical Design

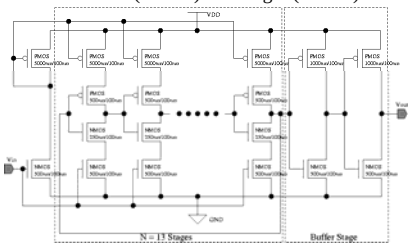
Current starved VCO design performed using 90nm generic process. Target oscillation frequency (*f0*)= 2GHz.

$$f_0 = \frac{I_D}{N * C_{tot} * V_{DD}}, \quad \text{.....(1)}$$

$$C_{tot} = \frac{5}{2} C_{ox} (W_p L_p + W_n L_n), \quad \text{.....(2)}$$

$$C_{ox} = \frac{\varepsilon_{r_{ox}} \varepsilon_0}{T_{ox}}, \quad \text{.....(3)}$$

V_{DD} : supply voltage, I_D: current flowing through inverter, N: odd number of inverters, C_{tot}: total capacitance of each inverter stage, C_{ox}: gate oxide capacitance per unit area, {Wp, Lp}: inverter PMOS width (500nm) and length (100nm), {Wn, Ln}: inverter NMOS width (250nm) and length (100nm), {Wpcs, Lpcs}: current starved PMOS width (5um) and length (100nm), {Wncs, Lncs}: current starved NMOS width (500nm) and length (100nm).



VCO Performance Optimization for Parasitics and Process Variations

- {V_{DD}, $V_{T,NMOS}$, $V_{T,PMOS}$, $T_{OX,NMOS}$, $T_{OX,PMOS}$} chosen as parameters for process variation.
- Parameters varied by +/-10% from their nominal values. Worst case identified in which V_{DD} is reduced by 10%, and process parameters are increased by 10%. In this case, a 43.5% discrepancy is observed between the logical and physical design.

Parameter	Unoptimized Physical Design	Unoptimized Physical Design + Process variation	Optimized Physical Design + Process Variation
frequency	$1.56GHz$	$1.13GHz$	$1.91GHz$
discrepancy	25%	43.5%	4.5%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (−10%)	$1.08V$
$V_{T,NMOS}$	$0.1692662V$ (nominal)	$0.186193V$ (+10%)	$0.186193V$
$V_{T,PMOS}$	$-0.1359511V$ (nominal)	$-0.149546V$ (+10%)	$-0.149546V$
$T_{ox,NMOS}$	$2.33nm$ (nominal)	$2.563nm$ (+10%)	$2.563nm$
$T_{ox,PMOS}$	$2.48nm$ (nominal)	$2.728nm$ (+10%)	$2.728nm$

Parasitic-aware netlist from first layout is parameterized, and subjected to optimization loop in circuit simulator. {Wp, Lp, Wn, Ln, Wpcs, Lpcs, Wncs, Lncs} constitute set of design variables.

Parameter	Varied from	Varied to	Optimized Value
W_n	$200nm$	$500nm$	$415nm$
W_p	$400nm$	$1\mu m$	$665nm$
W_{ncs}	$1\mu m$	$5\mu m$	$4\mu m$
W_{pcs}	$5\mu m$	$20\mu m$	$19\mu m$
L	$100nm$	$110nm$	$100nm$

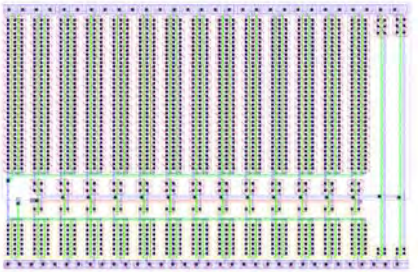
Using optimized design variables:
- Target $f_0 \geq 2$GHz.
- Logical design f_0 = 1.95GHz.
- Physical design f_0 in worst case process variation environment = 1.91 GHz.
- Physical design f_0 in nominal case process environment = 2.54 GHz.

Hence a final optimized layout with f_0 = 1.91GHz under worst case process variation is obtained with only 1 manual (layout) iteration.

VCO Physical Design

- Physical design carried out using a 90nm salicide 1.2V/ 2.5V 1 Poly 9 Metal process.
- Full extraction including resistors (R), capacitors (C), inductors (L) and mutual inductors (K) is performed.
- Multi-fingered transistors are laid out to minimize the area overhead.

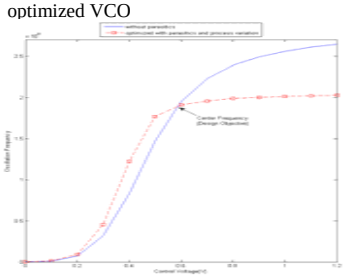
Final Optimized layout of the VCO



Measured Performance of the VCO

Parameter	Value
Technology	$90nm$ CMOS $1P$ $9M$
Supply Voltage (V_{DD})	$1.2V$
Oscillation frequency (Nominal process)	$2.54GHz$
Process and supply variation	V_T (+10%), T_{ox} (+10%), V_{DD} (−10%)
Oscillation frequency (Worst-case process)	$1.91GHz$
Number of design variables	5 (W_n, W_p, W_{ncs}, W_{pcs}, L)
Number of objectives	1 ($f_0 >= 2GHz$)

Frequency-voltage characteristics of the optimized VCO



Conclusions

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