A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-V_{DD} SoCs

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Abstract

- *Level Converters are becoming overhead for the circuits they are employed in. If their power consumption continues to grow, they will fail to serve their purpose.*
- *We propose the application of a dual-Tox (DOXCMOS) technique for power-delay optimization of a DC-DC voltage level converter. 83% power savings and 60% delay savings are achieved over existing designs. The proposed converter performs level-up/down conversion and blocking of input signal.*
- *The design is robust, producing stable output for voltages as low as 0.6V and loads varying from 10fF to 200fF. The entire design cycle has been carried out up to physical design, including parasitic re-simulation at 90nm technology. To the best of the authors' knowledge, this is the first ULC subjected to DOXCMOS technology for power-delay optimization.*

Introduction and Motivation

- Major components of total power dissipation are:

1. Switching power dissipation.
2. Short-circuit power dissipation.
3. Leakage power dissipation.

- Each power dissipation source is dependent on supply voltage (V_{dd}), some linearly and some quadratically.
- Level-down conversion is used for reducing switching power dissipation in a circuit where the non-critical blocks are operated at lower supply voltage.
- Level-up conversion is used as an interface where low V_{dd} cells (V_{ddl}) drive high V_{dd} cells (V_{ddh}), thereby reducing short-circuit power dissipation.
- Blocking is used to shut down unused blocks in standby mode.
- The proposed circuit performs all three functions, namely: level-up/down conversion and blocking of input signal. Hence, it is called a *Universal Level Converter* (ULC).

Total Power Dissipation in the ULC circuit (P_{ULC})

- Dynamic Power ($P_{dynamic}$)
- Sub-threshold Leakage ($P_{subthreshold}$)
- Gate Oxide Leakage ($P_{gate\text{-}oxide}$)

$$P_{dynamic} = \alpha C_L V_{dd}^2 f, \quad \text{.....(1)}$$

$$I_{sub} = \mu_0 \left(\frac{\varepsilon_{ox} W_{eff}}{T_{ox} L_{eff}}\right) v_{therm}^2 e^{1.8} \exp\left(\frac{V_{gs} - V_T}{v_{therm} S}\right)\left(1 - \exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right), \quad \text{.....(2)}$$

$$J_{DT} = A\left(\frac{V_{ox}}{T_{ox}}\right)^2 \exp\left(\frac{-B\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{\frac{3}{2}}\right)}{\left(\frac{V_{ox}}{T_{ox}}\right)}\right), \quad \text{.....(3)}$$

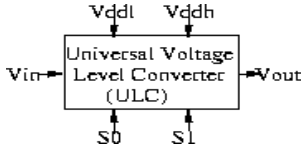
$$Delay \propto \left(\frac{C_L V_{dd}}{\mu\left(\frac{\varepsilon_{ox}}{T_{ox}}\right)\left(\frac{W_{eff}}{L_{eff}}\right)(V_{dd} - V_T)^{\alpha}}\right), \quad \text{.....(4)}$$

$$Delay_{ULC} = \left(\frac{Delay_{up} + Delay_{down}}{2}\right), \quad \text{.....(5)}$$

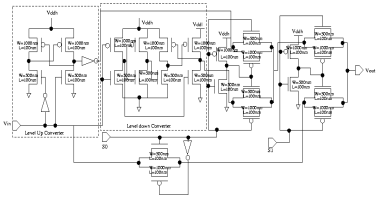
α: activity factor, C_L: capacitive load, f: clock frequency, I_{sub}: subthreshold current in transistor, ε_0: gate oxide dielectric constant, L_{eff}: effective channel length, W_{eff}: effective channel width, V_T: threshold voltage, vtherm: thermal voltage, S: subthreshold swing factor, V_{gs}: gate-source voltage, V_{ds}: drain-source voltage, T_{ox}: gate-oxide thickness, J_{DT}: direct tunneling current density, V_{ox}: potential drop across thin oxide, φ_{ox}: barrier height for tunneling particle (electron or hole), {A,B}: physical parameters, μ: electron surface mobility, α: velocity saturation index.

ULC Transistor Level Design

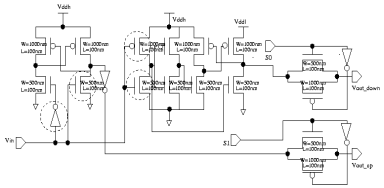
The ULC consists of input voltage signal (Vin), control signals (S1 and S0), supply voltages (Vddl and Vddh) and output voltage signal (Vout).



- Level-up conversion performed using CCLC (Cross coupled level converter) circuit.
- Level-down conversion performed using differential input level converter.



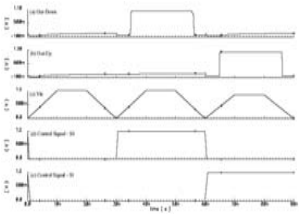
Baseline design with 32 transistors.



Area optimal design with 24 transistors. The power-hungry transistors are circled.

Select Signal		Type of Operation
S1	S0	
0	0	Block Signal
0	1	Down Conversion
1	0	Up Conversion

Functionality Truth Table for the area optimal design.



Functional simulation of area optimal ULC following truth table.

Power-Delay Optimal Design

To optimize power and delay, the following parameters are varied:

- T_{ox} of power hungry NMOS transistors.
- T_{ox} of power hungry PMOS transistors.
- Width ($W_{NMOSdown}$) of NMOS transistors of down converter.
- Width ($W_{PMOSdown}$) of PMOS transistors of down converter.
- Width (W_{NMOSup}) of NMOS transistors of up converter.
- Width (W_{PMOSup}) of PMOS transistors of up converter.

Optimized values of power and delay obtained are:

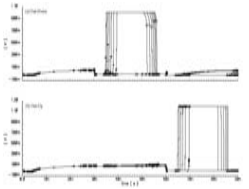
- P_{ULC} = 16.68μW.
- $Delay_{up}$ = 80.35ps.
- $Delay_{down}$ = 80.43ps.
- $Delay_{ULC}$ = 80.39ps.

Final values of optimization parameters:

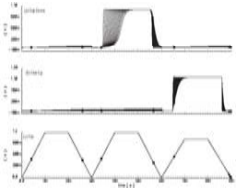
- Tox of power-hungry NMOS transistors =2.667nm (14% increase from nominal).
- Tox of power-hungry PMOS transistors =3.624nm (32% increase from nominal).
- $W_{NMOSdown}$ = 120nm.
- $W_{PMOSdown}$ = 298.9nm.
- W_{NMOSup} = 428.3nm.
- W_{PMOSup} = 220.1nm.

83% power savings compared to the baseline design and 60% delay savings compared to existing designs have been obtained.

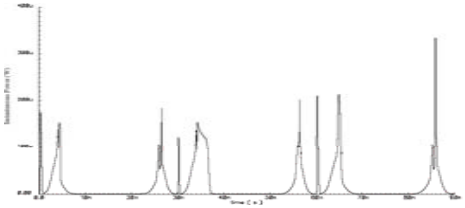
ULC Characterization



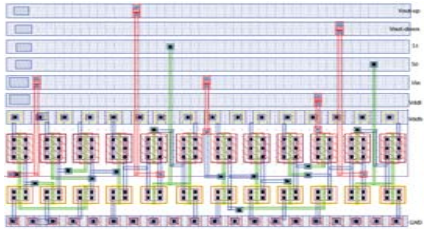
Parametric analysis with input voltage sweep.



Performance of the ULC under varying output capacitive load (10fF to 200fF).



Instantaneous power plot with C_L = 45fF.



Area optimal physical design of the ULC for 90nm technology.

Conclusions and Future Work

- We propose a DOXCMOS approach along with transistor geometry variations to reduce power-delay overhead of Universal Level Converter.
- Robustness of ULC is tested using parametric, load and power analysis. The design is area optimal. The physical design is also presented.
- This design will be re-implemented at 45nm node. Layout rules will be scaled from 90nm to 45nm. Efforts are also going on to include the block functionality in the level converter design itself.

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