Metrics to Quantify Steady and Transient Gate Leakage in Nanoscale Transistors: NMOS Vs. PMOS Perspective

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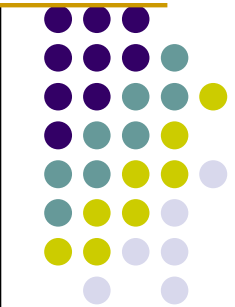
Outline of the Talk



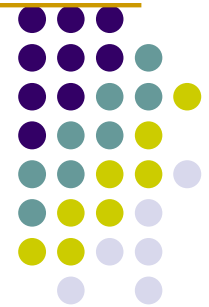
- CMOS scaling –Trends and Effects
- Leakage dissipation in Nano-CMOS
- Gate leakage analysis – 3 Proposed Metrics
- Impact of process variation on the metrics
- Monte Carlo Simulations: Modelling Variations
- Summary and Conclusions

Nano-CMOS Based Systems

? Energy costs, Battery life, Cooling costs

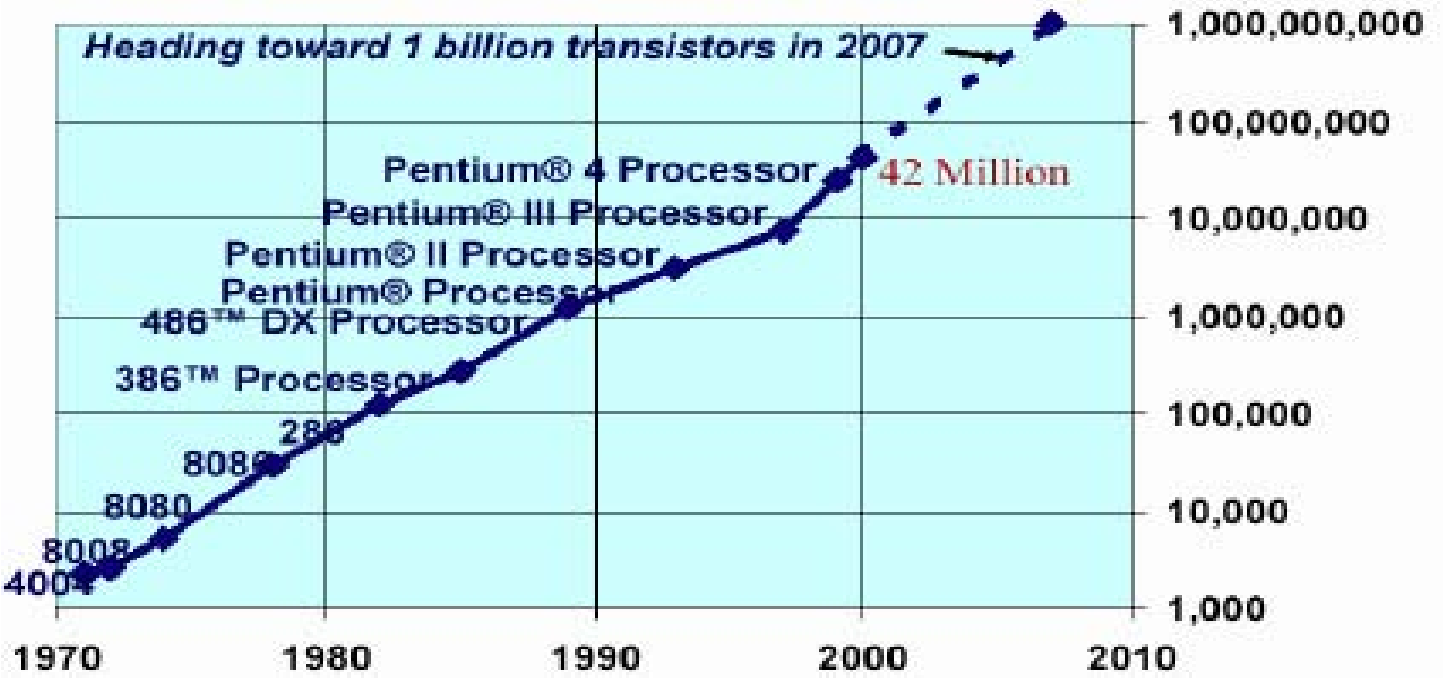
Power Analysis and Optimization

Almost the entire electronic appliance industry today is driven by CMOS technology.

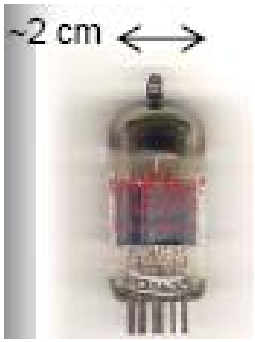


CMOS Technology Scaling and Leakage Dissipation

Scaling Trend – Transistor Count



Increase in Transistor Count per chip

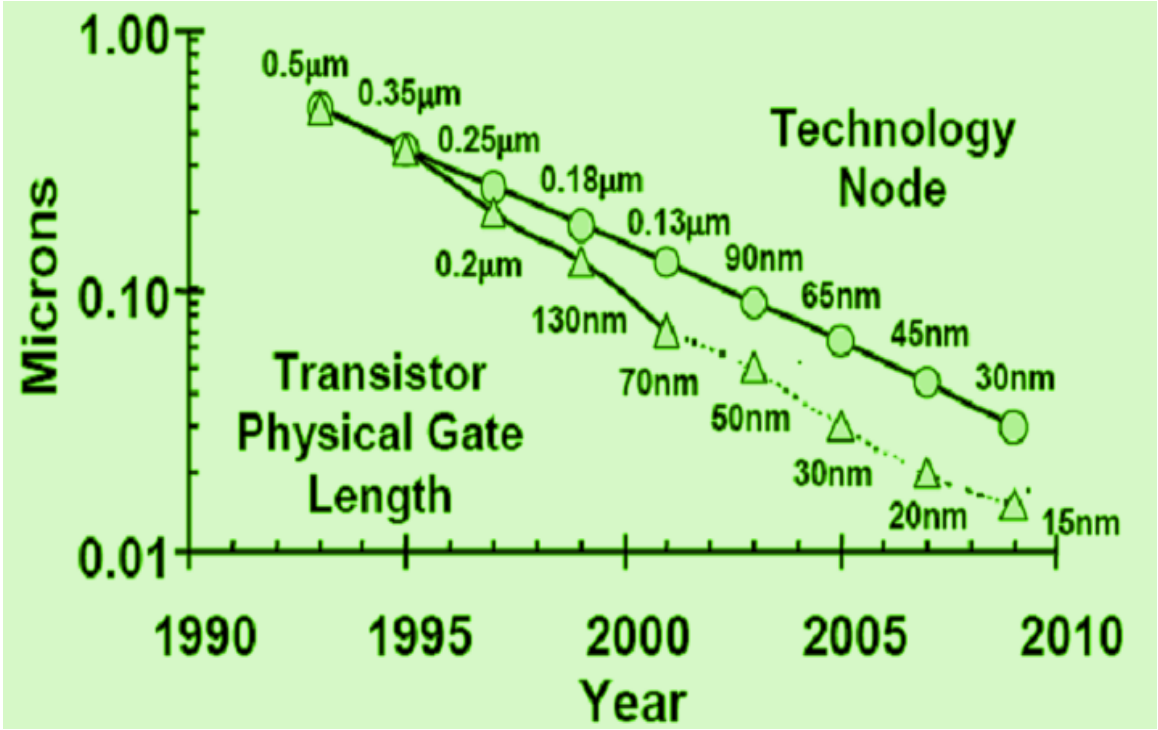


1967

VLSI technology is the fastest growing technology in the human history.

2007

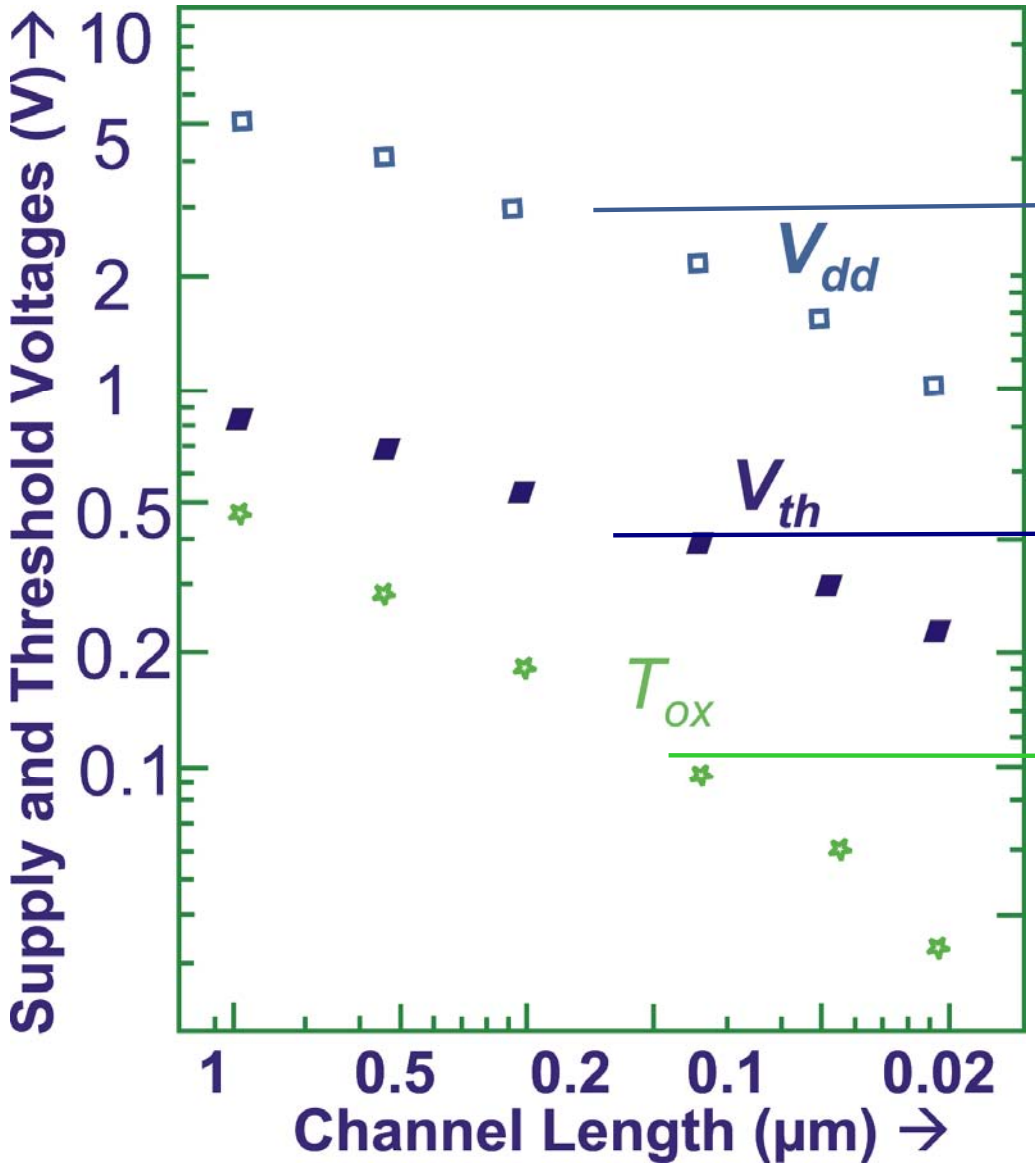
What is Physically Scaled? (Gate Length)



- Gate length of the transistor has been decreasing with technology scaling.
- All the other dimensions including gate oxide thickness have been scaled down to support this trend.

Source: Pedram ASPDAC 2004, Osburn IBM JRD Mar2002

Other Parameters Scaled?



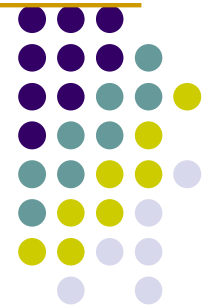
Supply Voltage

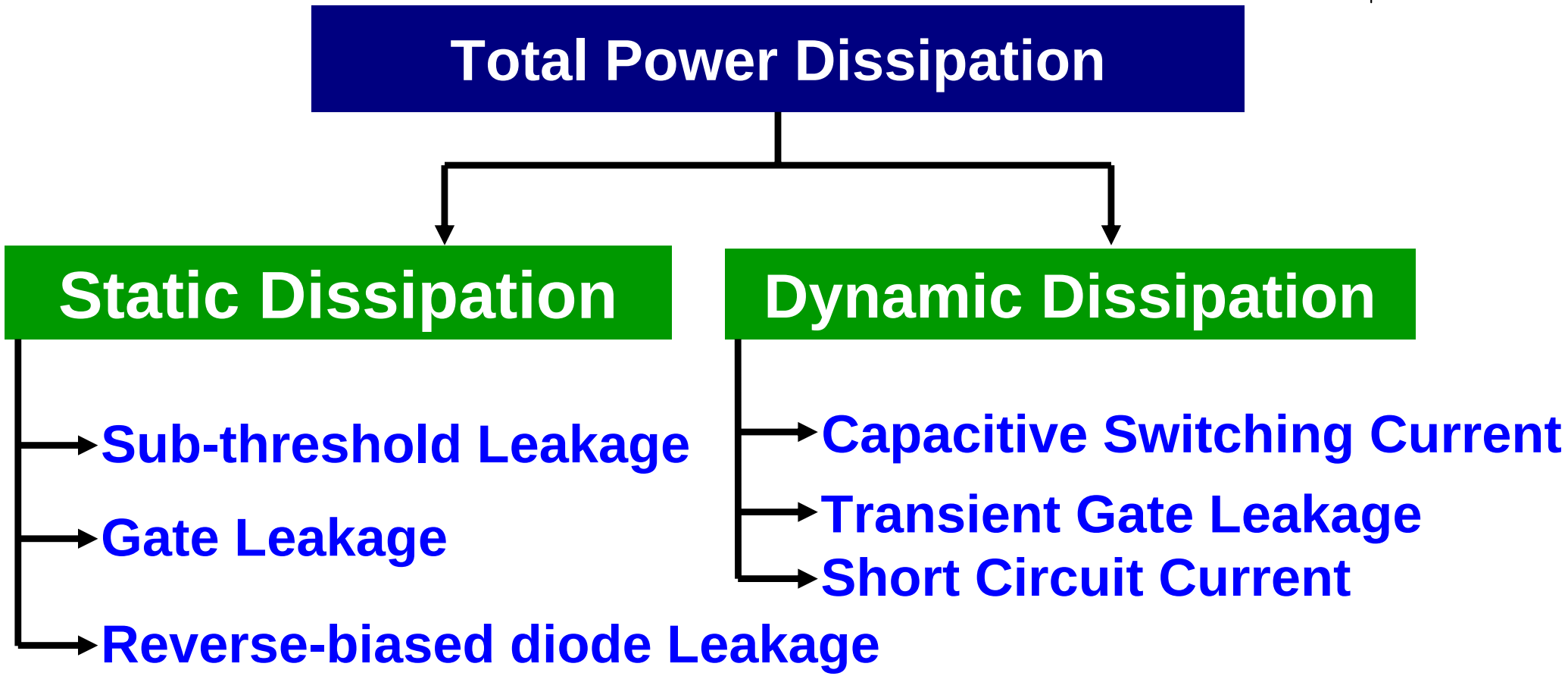
Threshold Voltage

Gate Oxide Thickness

Source: Taur IBM JRD MAR 2002

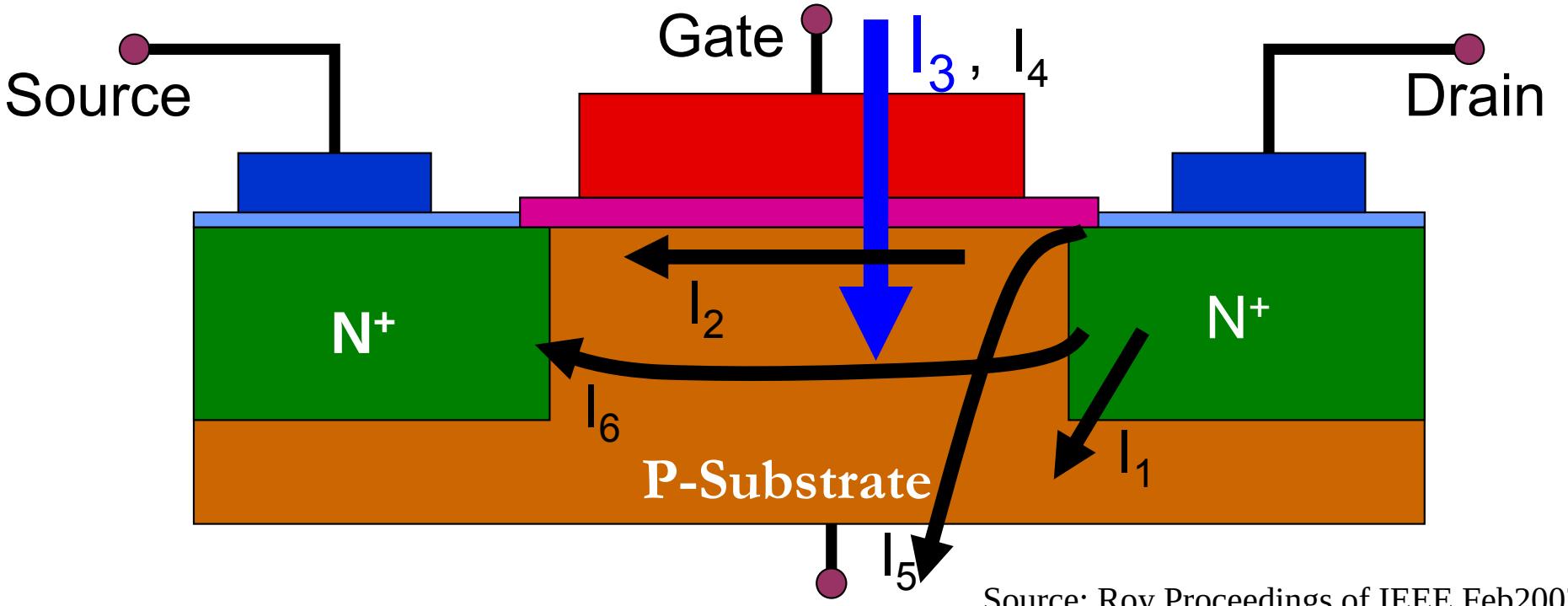
Power Dissipation in Nano-CMOS



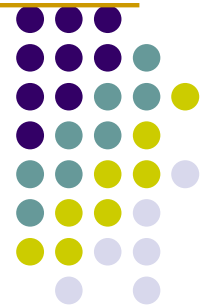


Leakages in Nanoscale CMOS

I_1 : reverse bias pn junction (both ON & OFF)
I_2 : subthreshold leakage (OFF)
I_3 :oxide tunneling current (both ON & OFF)
I_4 : gate current due to hot carrier injection (both ON & OFF)
I_5 : gate induced drain leakage (OFF)
I_6 : channel punch through current (OFF)

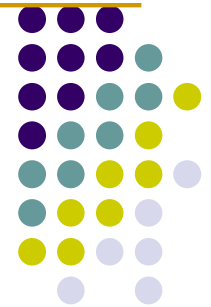


Source: Roy Proceedings of IEEE Feb2003



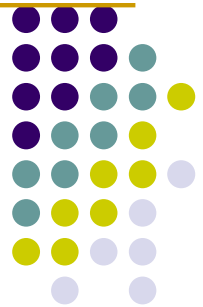
Contributions of Our Paper and Related Research

Contributions of Our Paper



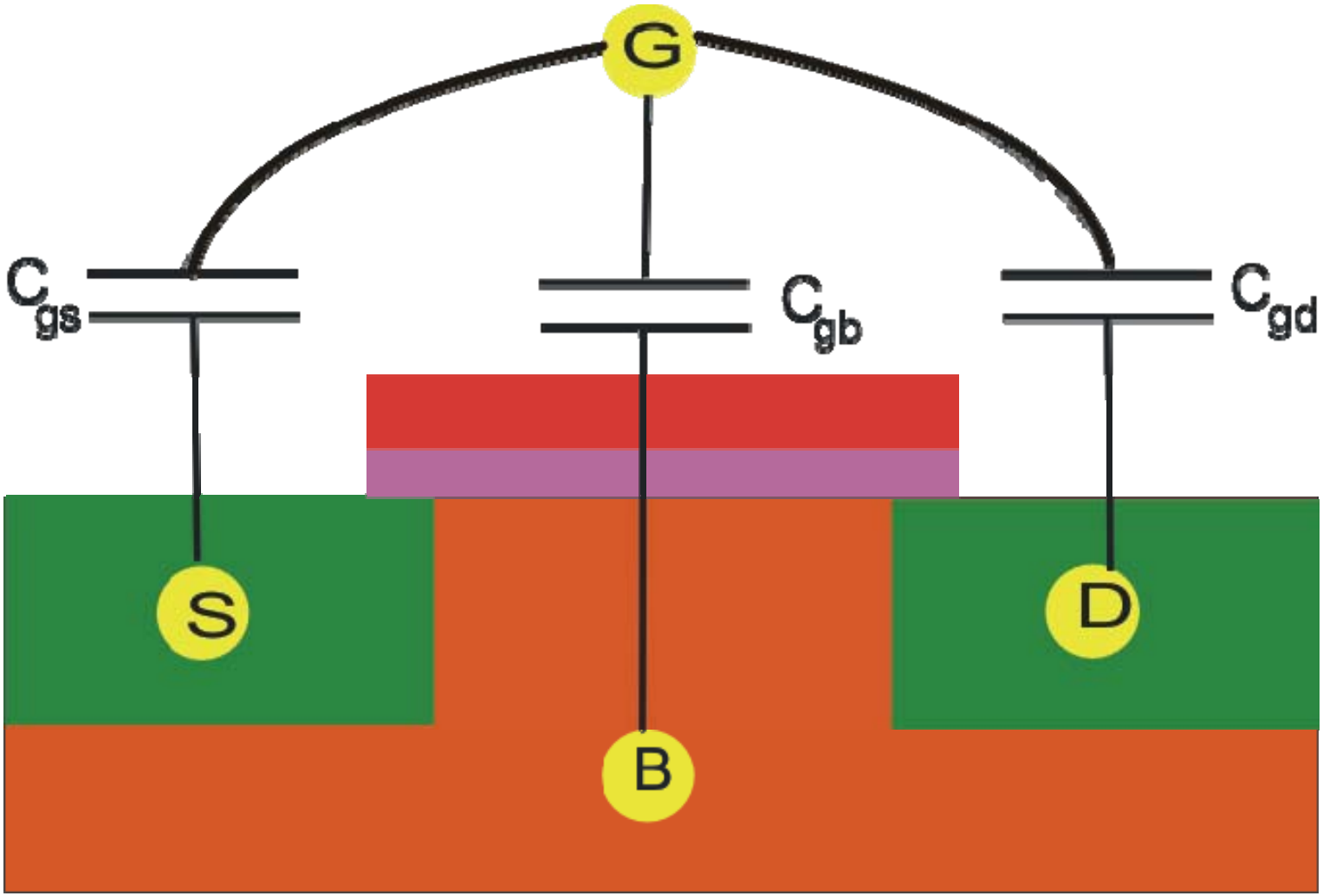
1. Both ON and OFF state gate leakage are significant.
2. During transition of states there is transient effect is gate tunneling current.
3. Three metrics: $I_{ON,}$ $I_{OFF,}$ and $C_{tunneling}$
4. $C_{tunneling}$: Manifests to intra-device loading effect of the tunneling current.
5. NMOS Vs PMOS in terms of three metrics.
6. Study process/supply variation on three metrics.

Contributions of Our Paper (Salient Feature)

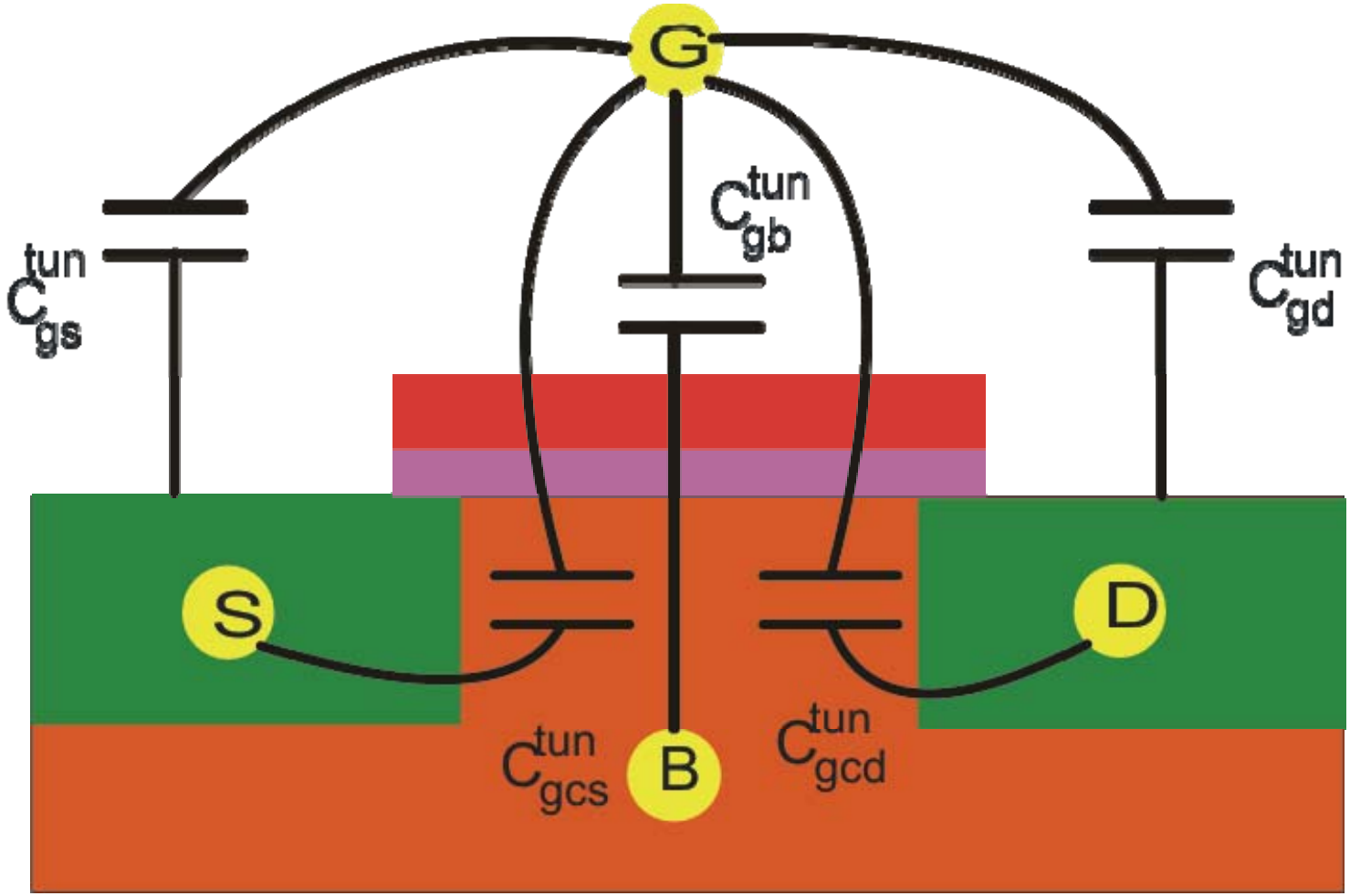


The metric, effective tunneling capacitance essentially quantifies the intra-device loading effect of the tunneling current and also gives a qualitative idea of the driving capacity of a Nano-CMOS transistor.

Gate Capacitance of a Transistor (Intrinsic)

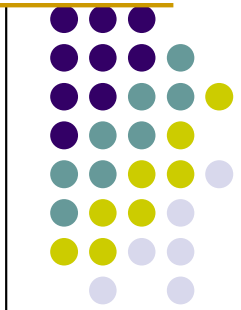


Gate Capacitance of a Transistor (Tunneling: Proposed)



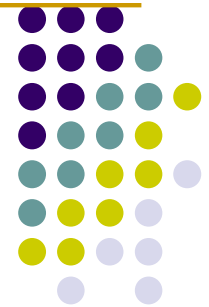
We propose that transient in gate tunneling current due to state transitions are manifested as capacitances.

Related Research Works (Gate Leakage Analysis)



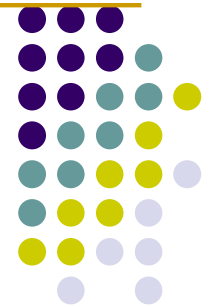
- Ghibaudo 2004: Characterization and modeling issues of ultra thin oxide devices
- Mukhopadhyay 2003: Characterization methodology is proposed along with reduction
- Yang 1999: Direct tunneling current and CV measurements in MOS devices used to model
- Hertani 2005: Provide leakage analysis of NAND, NOR, XOR gates

Related Research Works



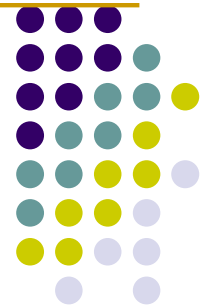
- No work characterize both ON and OFF
- No work examine the device or a logic gate when it changes stated:

  ON→OFF or OFF→ ON



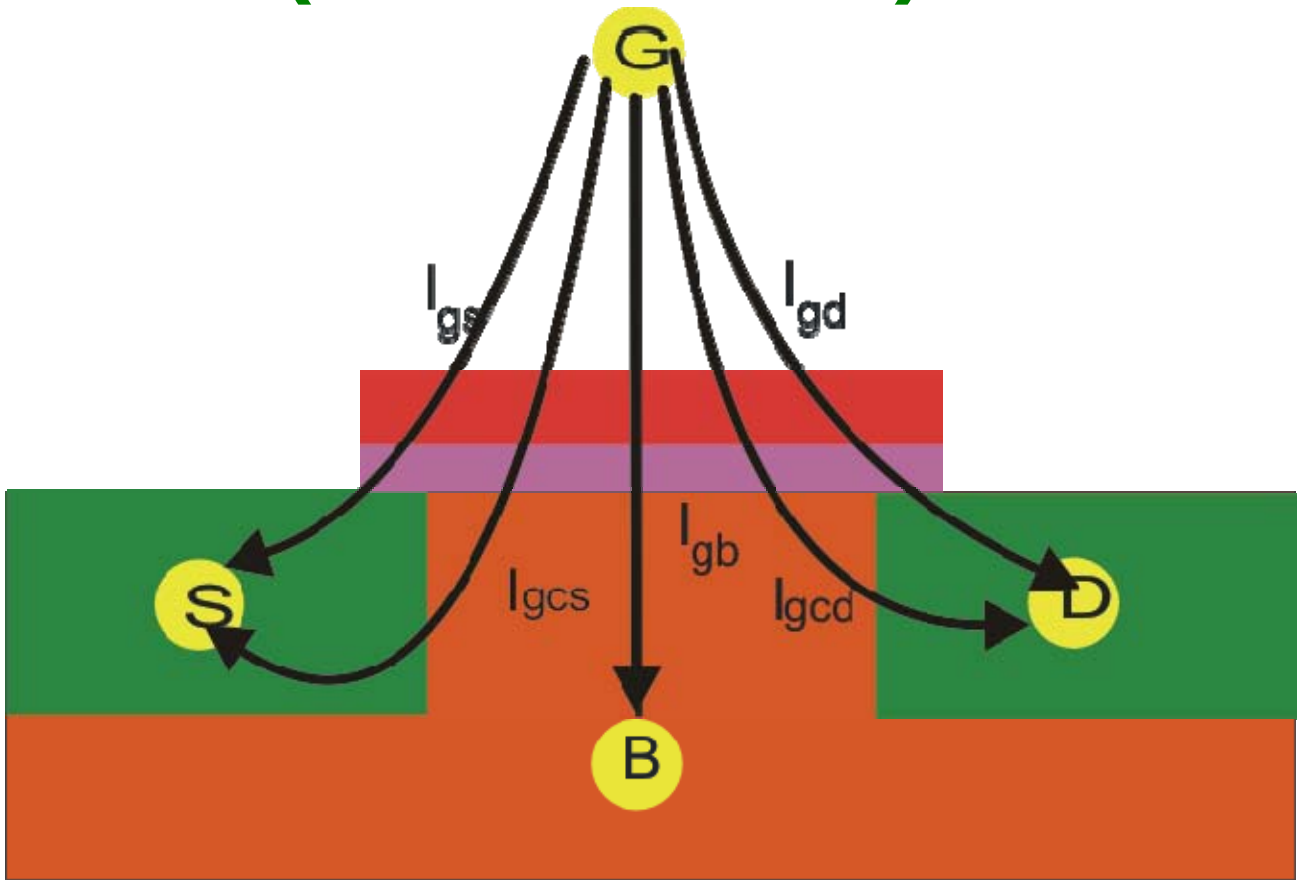
Analysis in a Nano-CMOS Transistor

Outline: Nano-CMOS Transistor



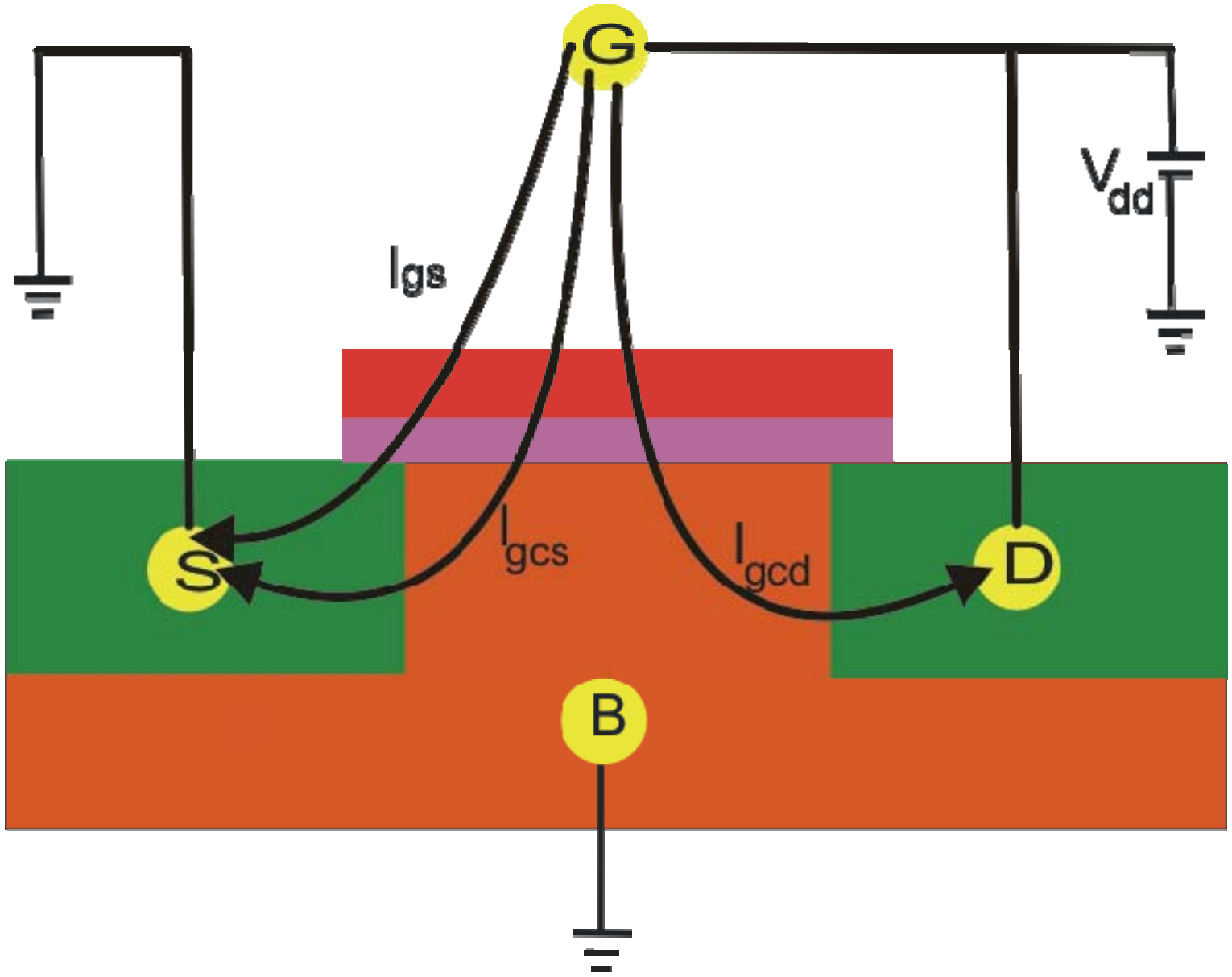
- Dynamics of gate oxide tunneling in a transistor
- SPICE model for gate leakage
- ON, OFF, and transition states of a transistor
- Gate leakage in ON, OFF, and transition states of a transistor

Gate Leakage Components (BSIM4 Model)

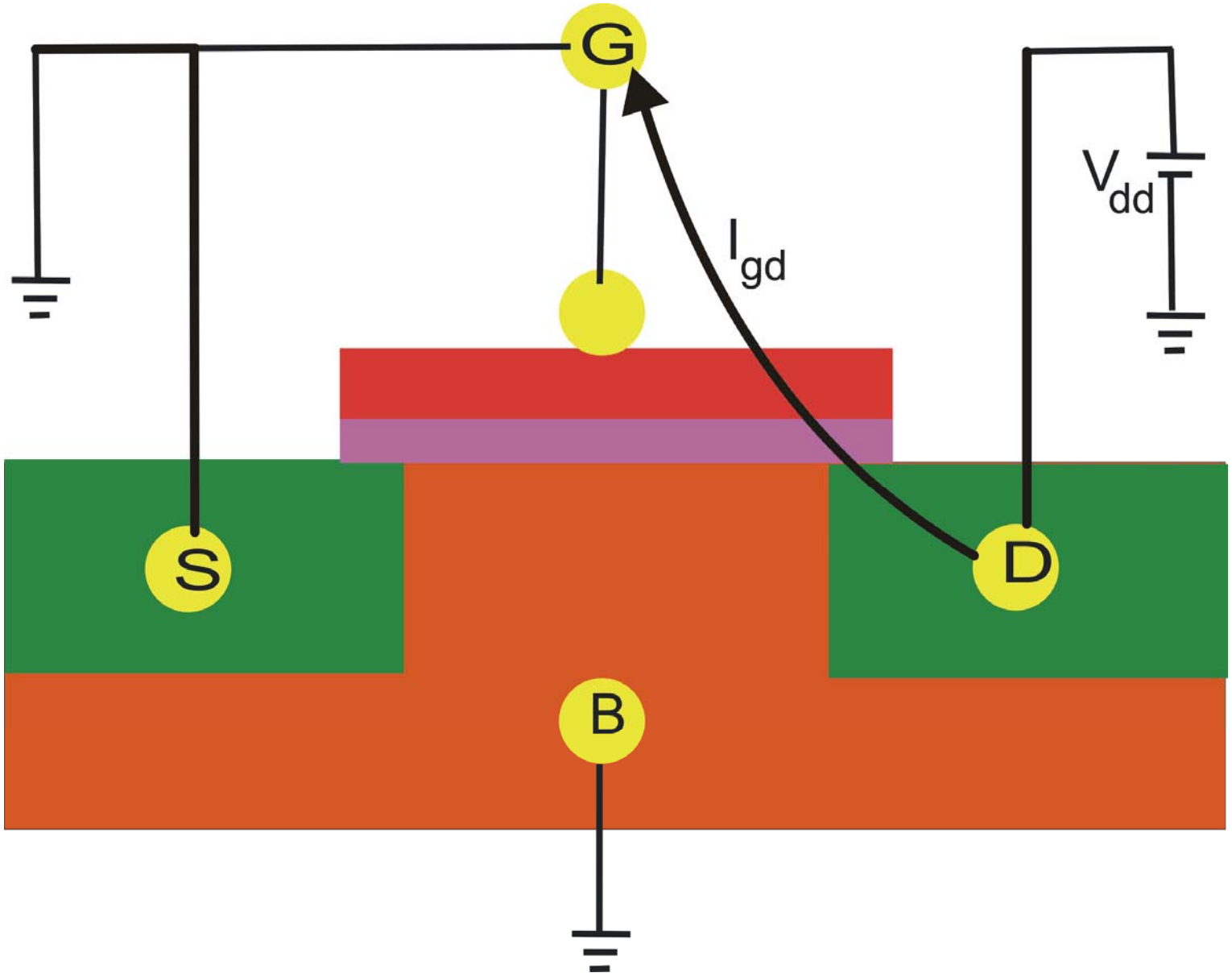


- I_{gs}, I_{gd}: tunneling through overlap of gate and diffusions
- I_{gcs}, I_{gcd}: tunneling from the gate to the diffusions via channel
- I_{gb}: tunneling from the gate to the bulk via the channel

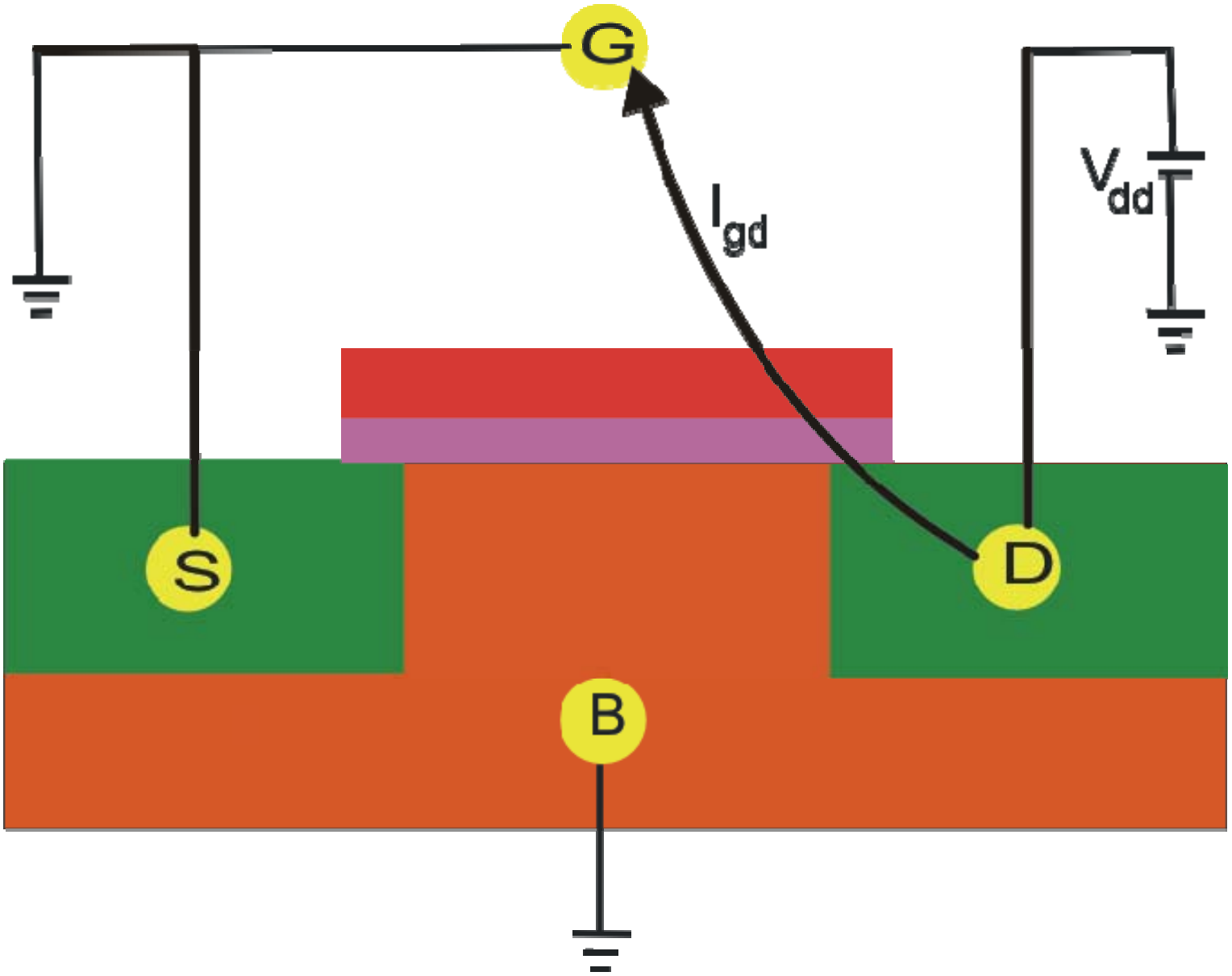
ON State: NMOS Transistor



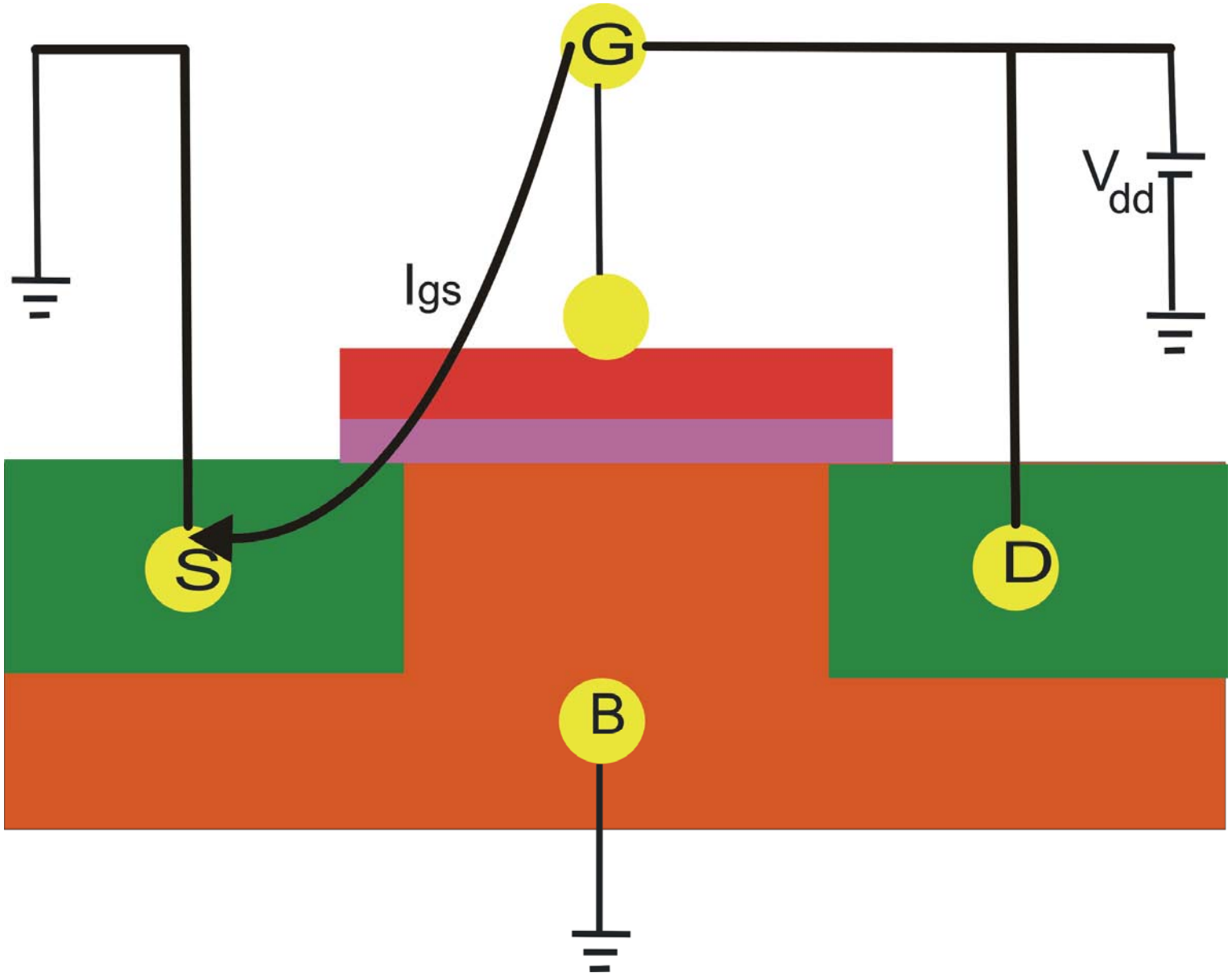
ON State: PMOS Transistor



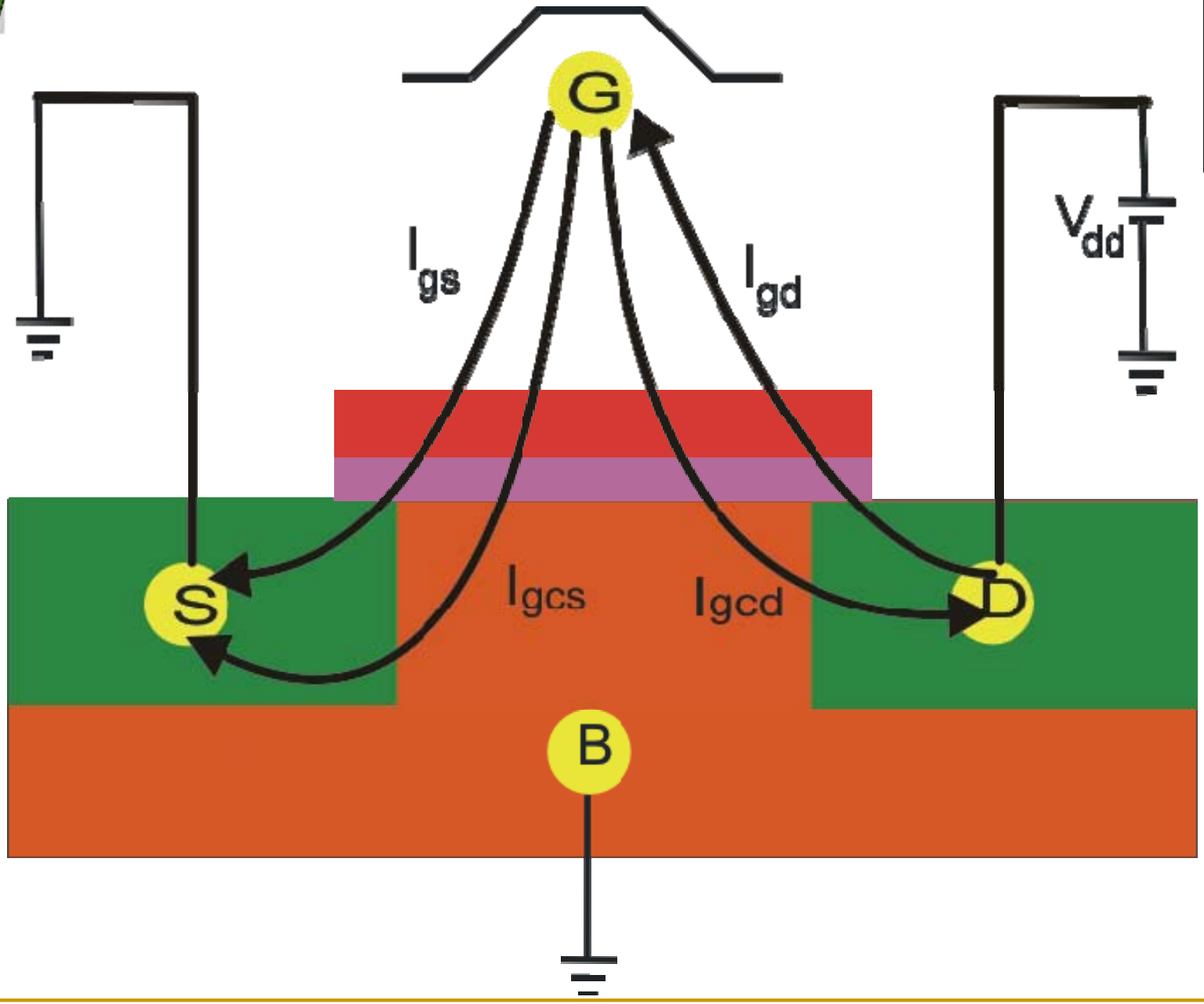
OFF State: NMOS Transistor



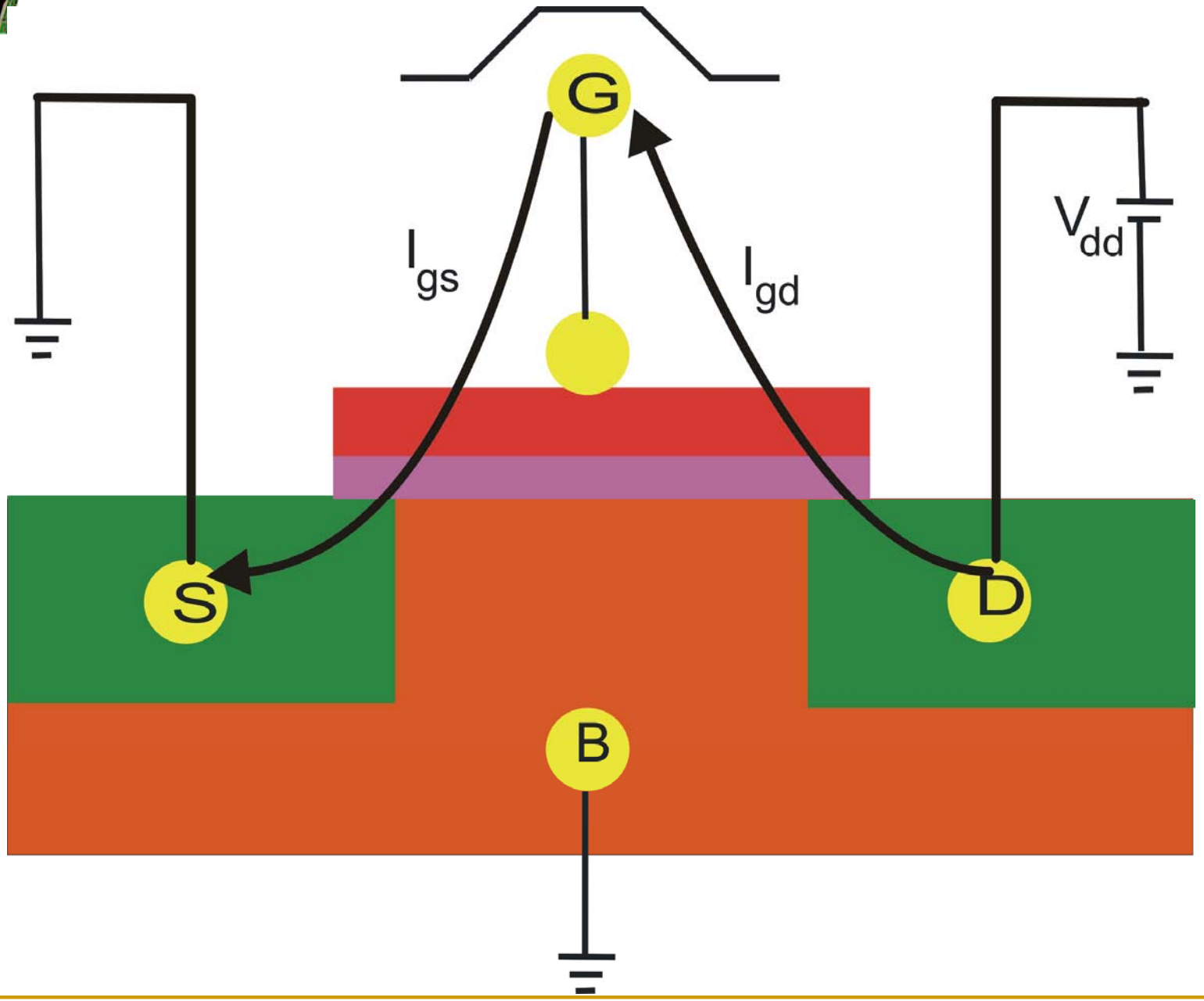
OFF State: PMOS Transistor



Transition State: NMOS Transistor



Transition State: PMOS Transistor



NMOS Gate Leakage Current (For a Switching Cycle)

Fig. 1

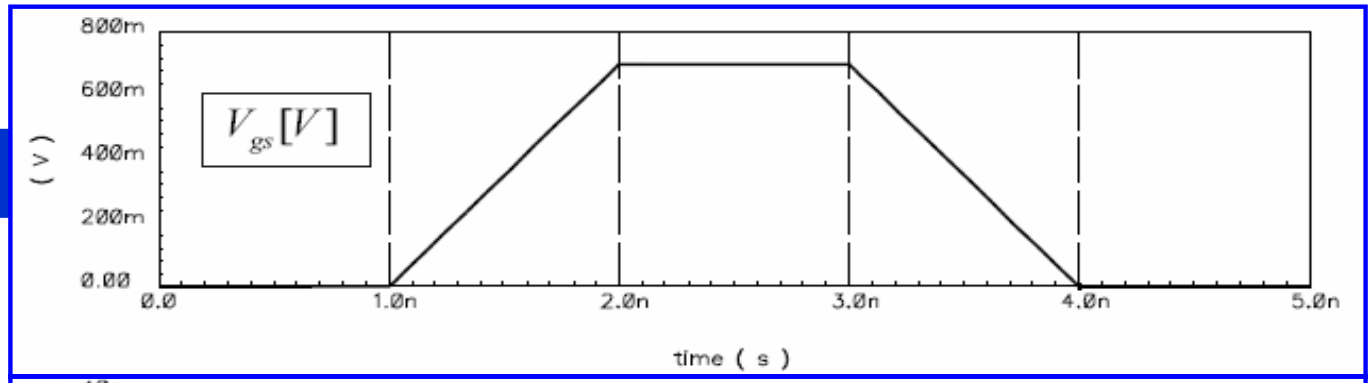
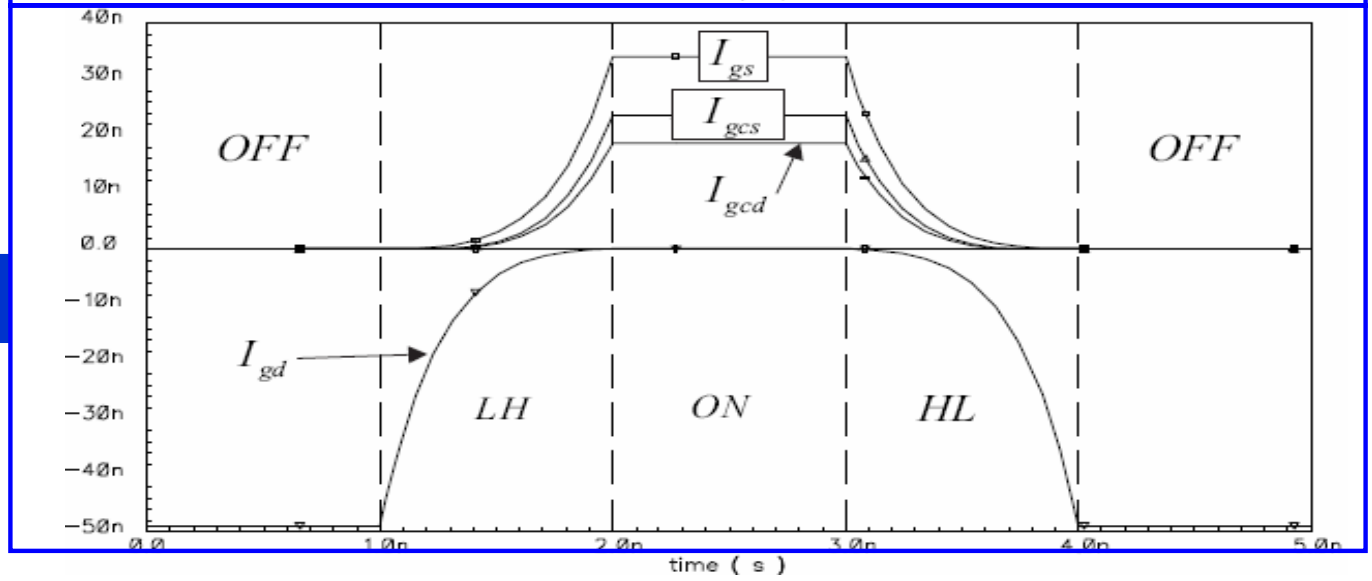


Fig. 2



PMOS Gate Leakage Current (For a Switching Cycle)

Fig. 1

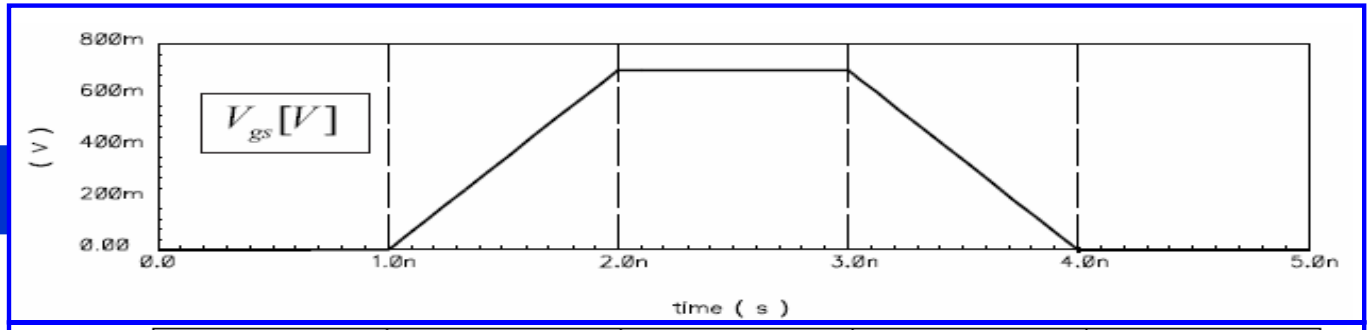
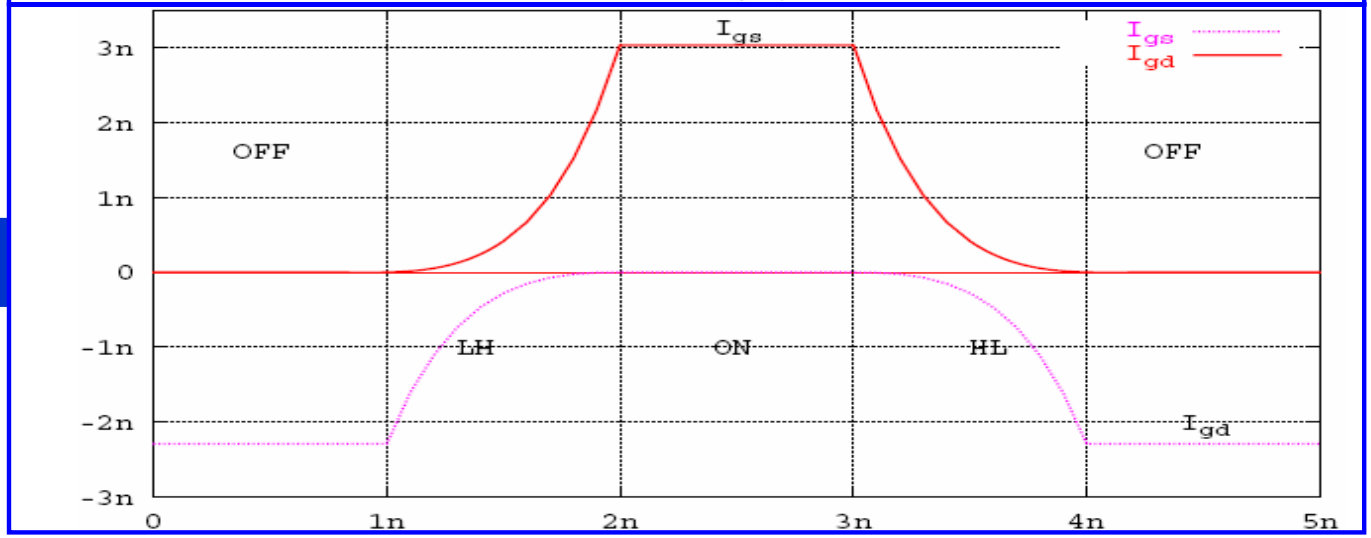
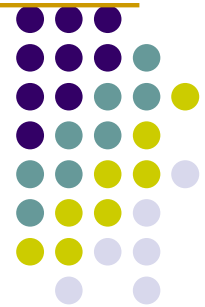


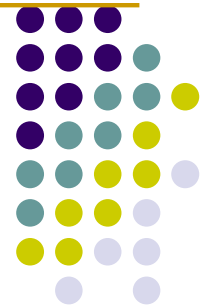
Fig. 2





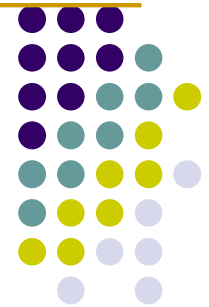
Three Metrics for Tunneling Current

Gate Leakage: Observation



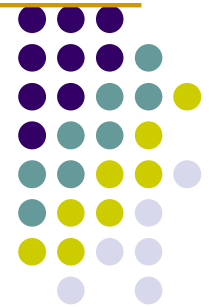
The behavior of the device in terms of gate tunneling leakage must be characterized not only during the steady states but also during transient states.

Gate Leakage: Metrics



- Gate leakage happens in ON state: I_{ON}
- Gate leakage happens in OFF state: I_{OFF}
- Gate leakage happens during transition: C_{eff}^{tun}

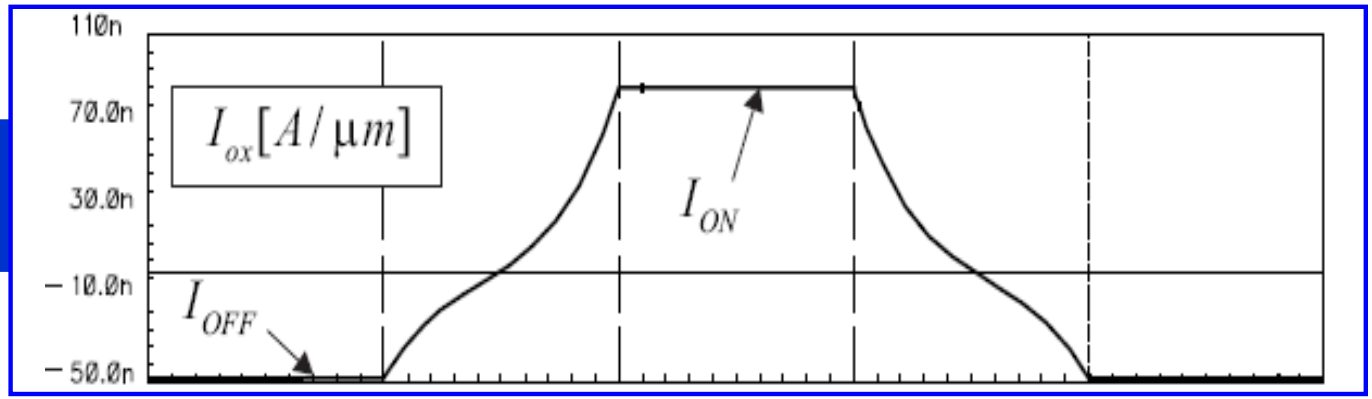
Gate Leakage for a Transistor



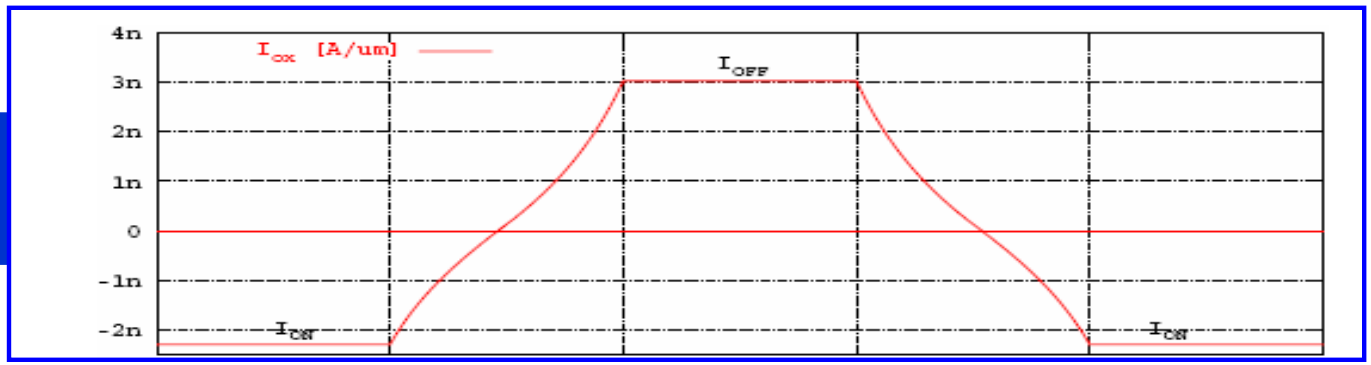
- Calculated by evaluating both the source and drain components
- For a MOS, $I_{ox} = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$
- Values of individual components depends on states: ON, OFF, or transition

Gate Leakage Current (For a Switching Cycle)

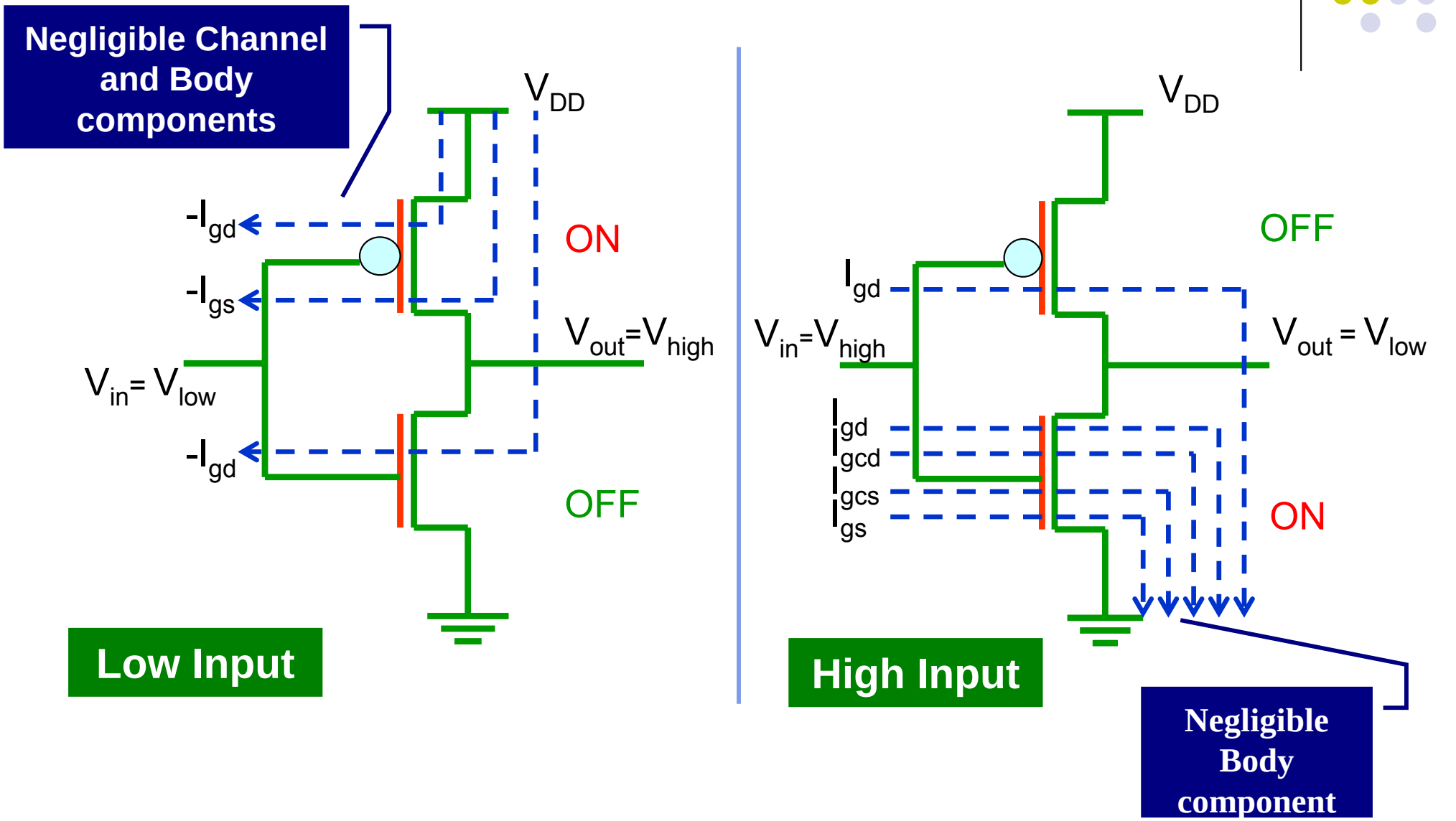
For NMOS



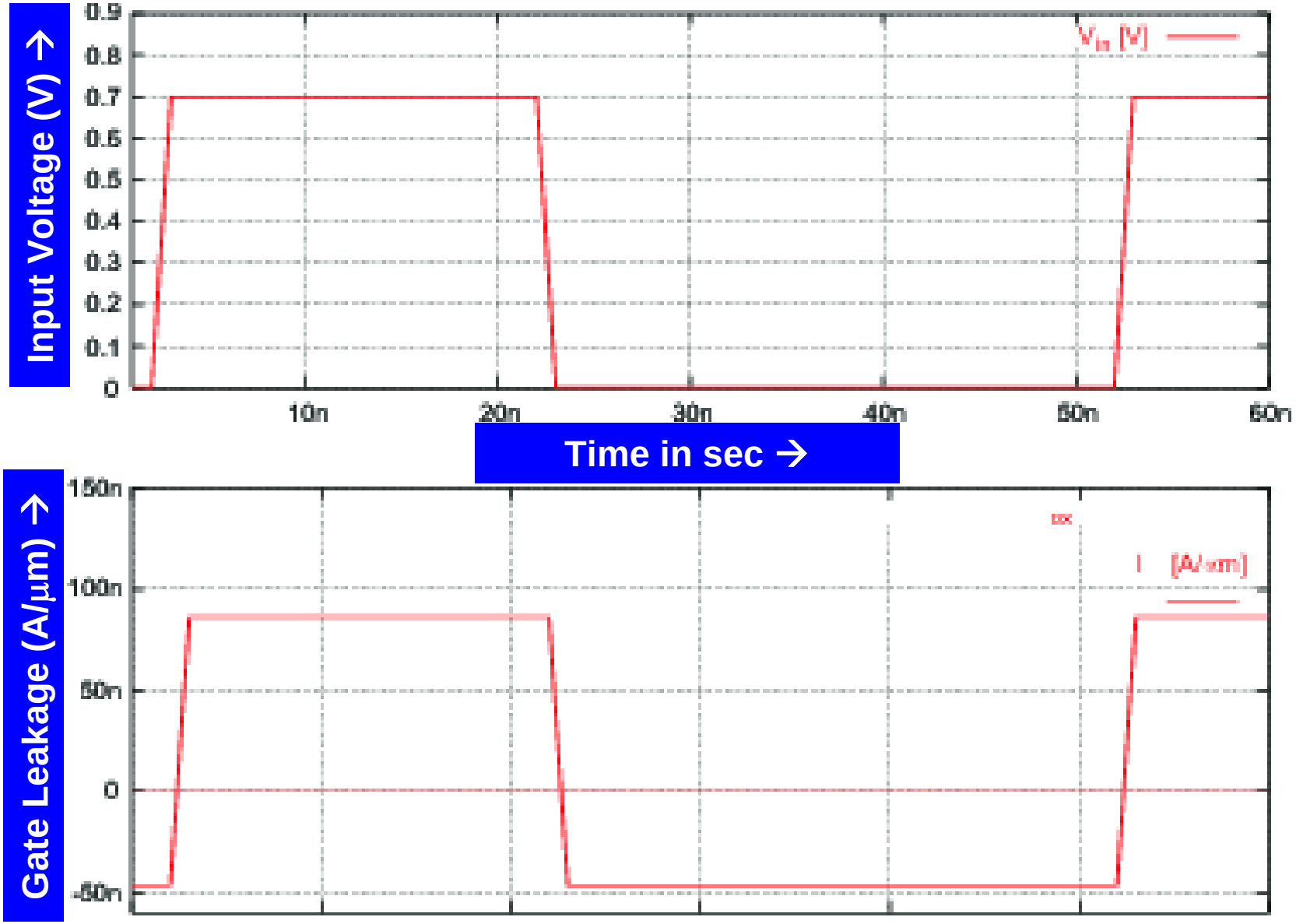
For PMOS



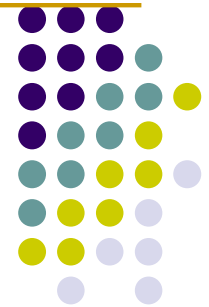
Inverter: Gate Leakage Paths (Putting NMOS and PMOS together)



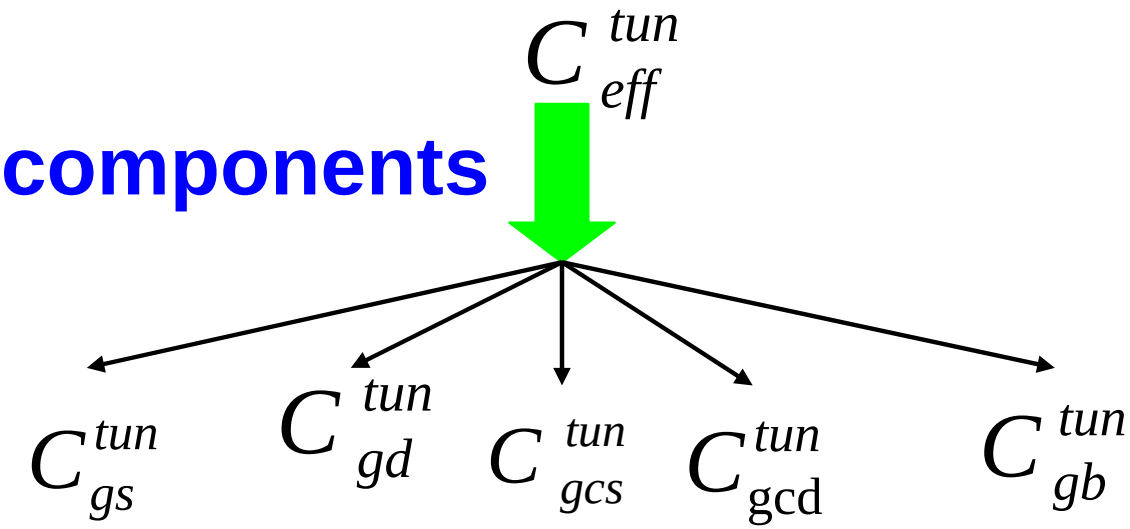
Inverter: Gate Leakage Current (For a Switching Cycle)



Transient Gate Leakage: C_{eff}^{tun}



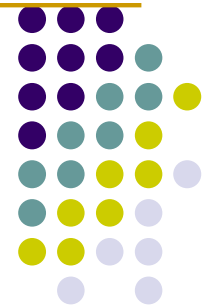
5 components



We propose to quantify as:

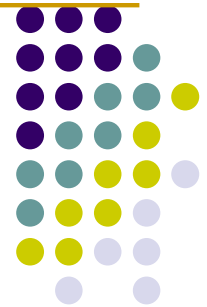
$$C_{eff}^{tun} = \frac{I_{ON} - I_{OFF}}{\left(\frac{dV_g}{dt}\right)}$$

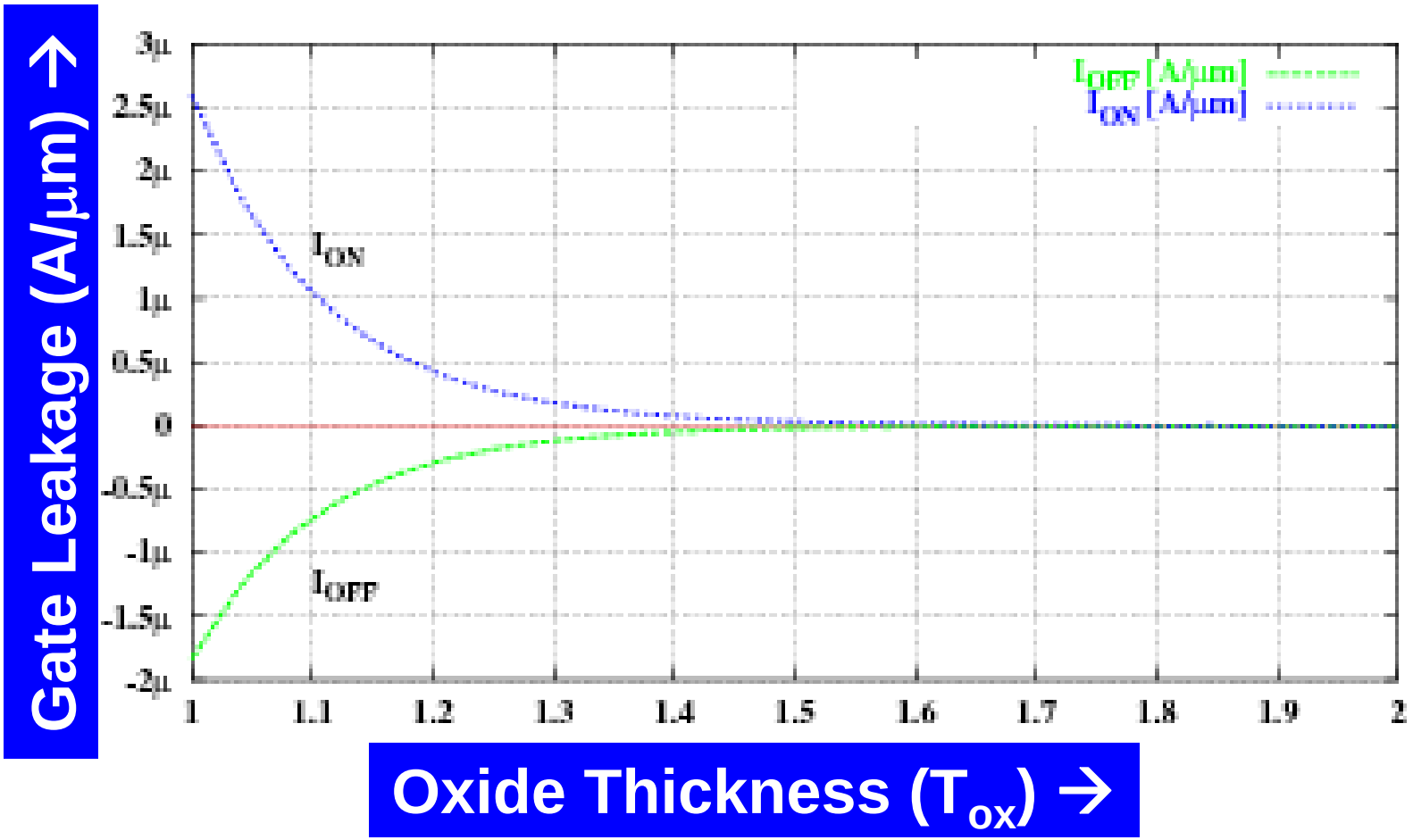
$$= \frac{I_{ON} - I_{OFF}}{V_{DD}} t_r$$ **(for equal rise/fall time)**



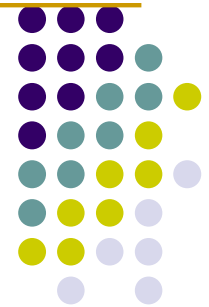
Effect of Process and Design Parameter Variation

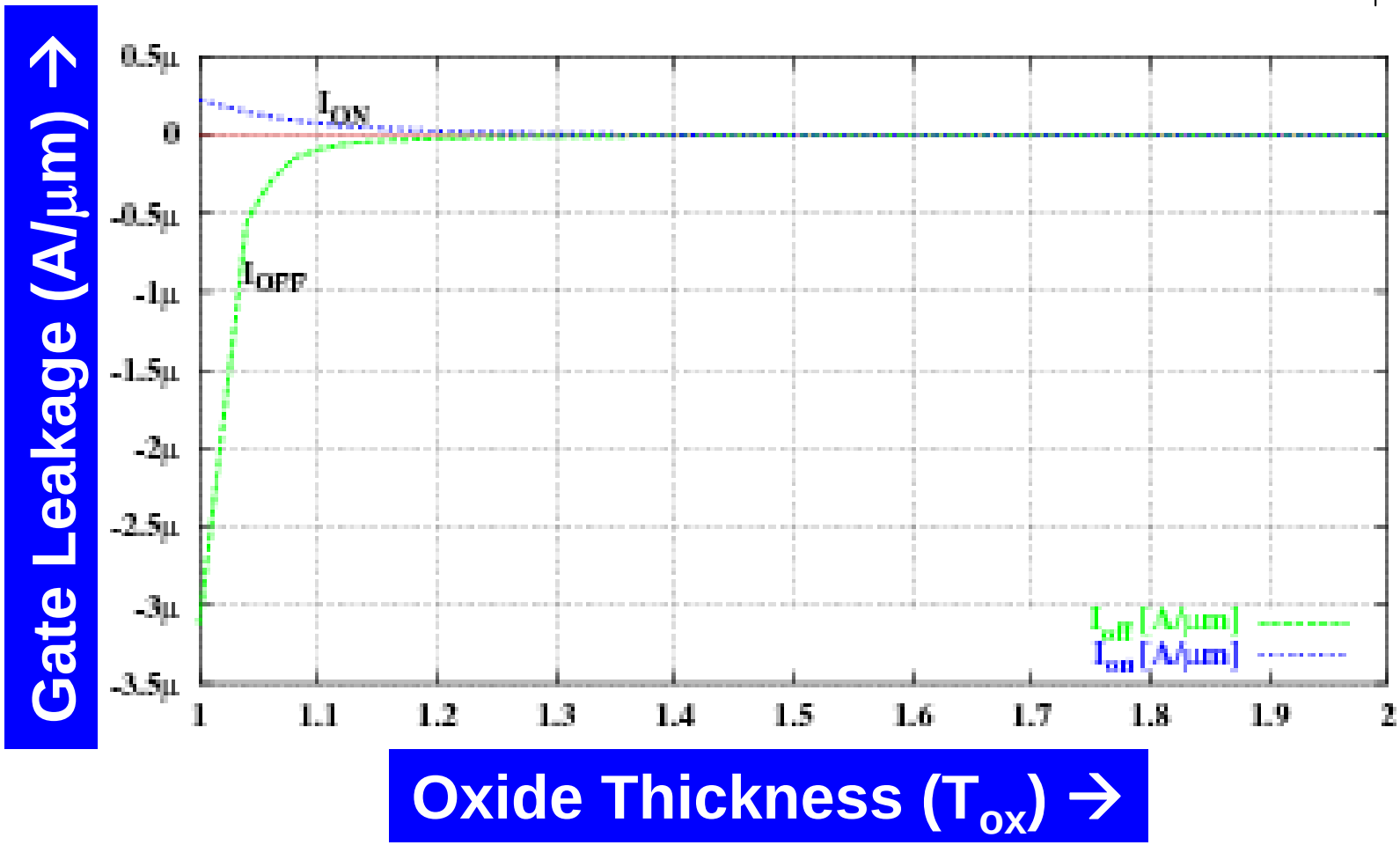
I_{ON} / I_{OFF} Versus T_{ox}: NMOS



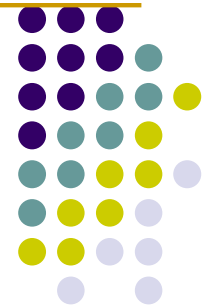


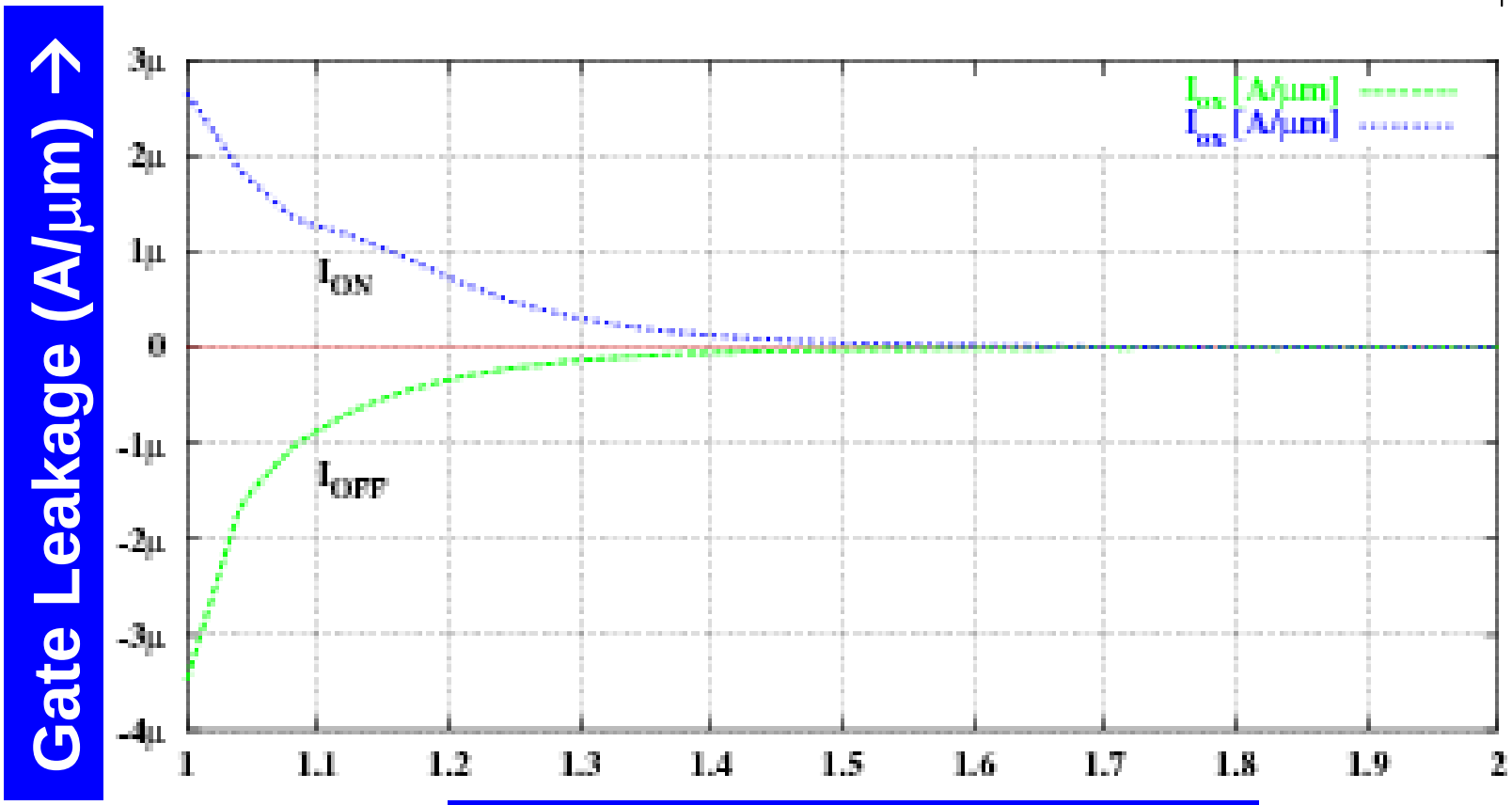
I_{ON} / I_{OFF} Versus T_{ox}: PMOS



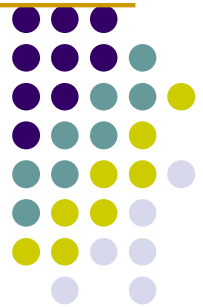


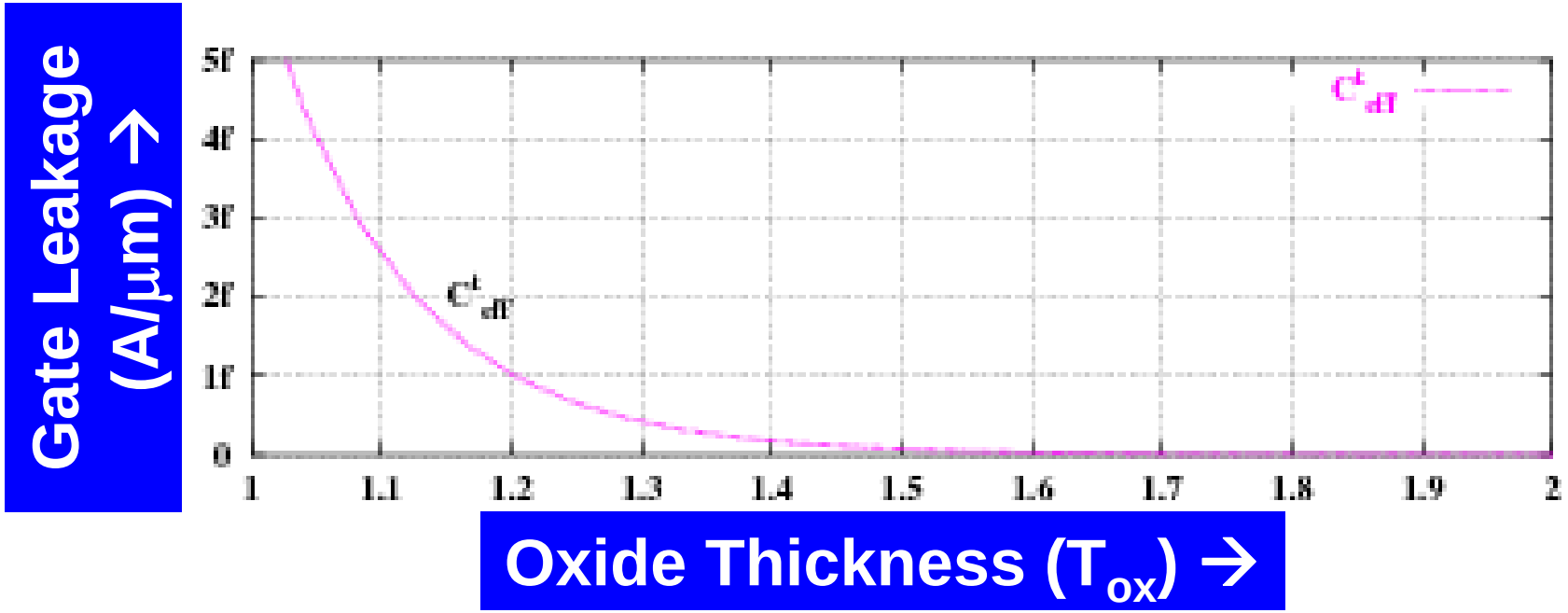
I_{ON} / I_{OFF} Versus T_{ox}: Inverter



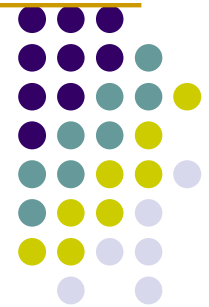


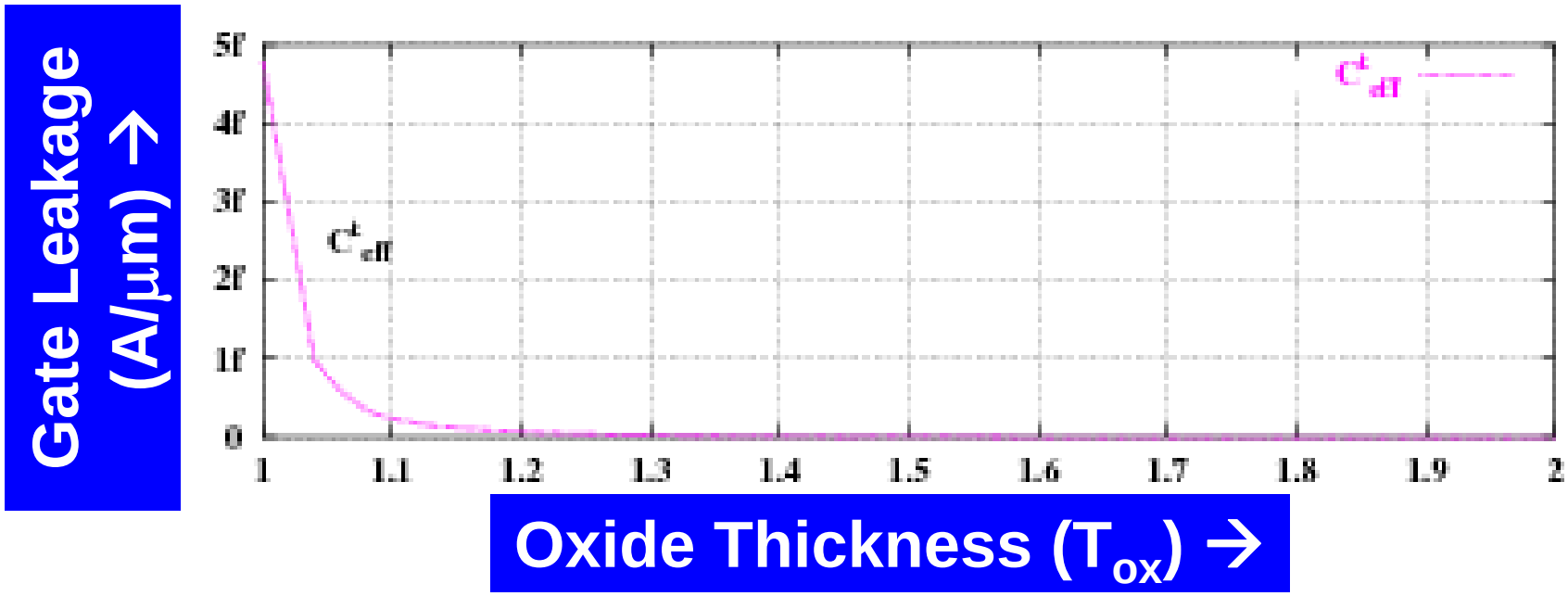
C_{eff}^{tun} Versus T_{ox}: NMOS



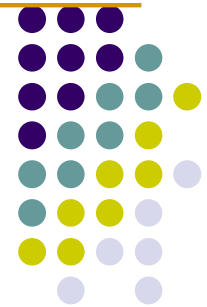


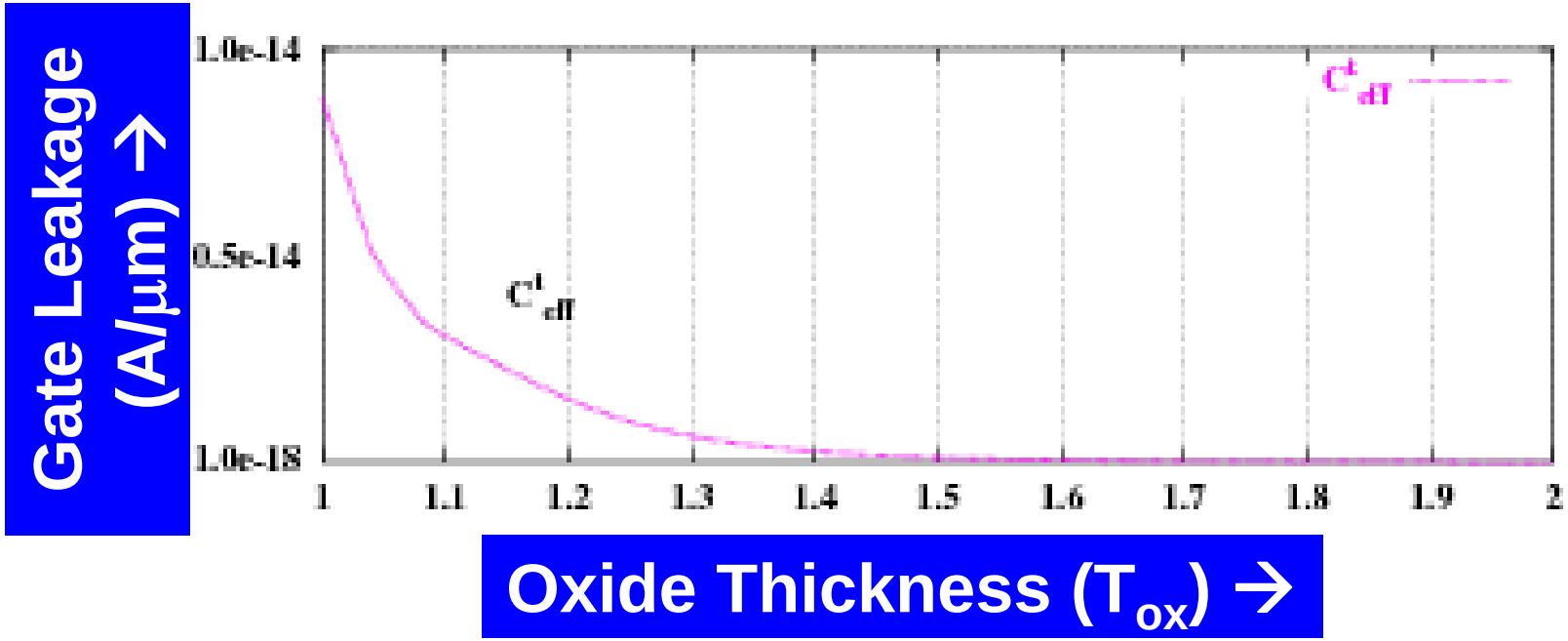
C_{eff}^{tun} Versus T_{ox}: PMOS

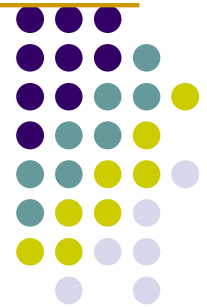




C_{eff}^{tun} Versus T_{ox}: Inverter

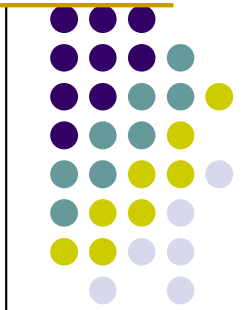




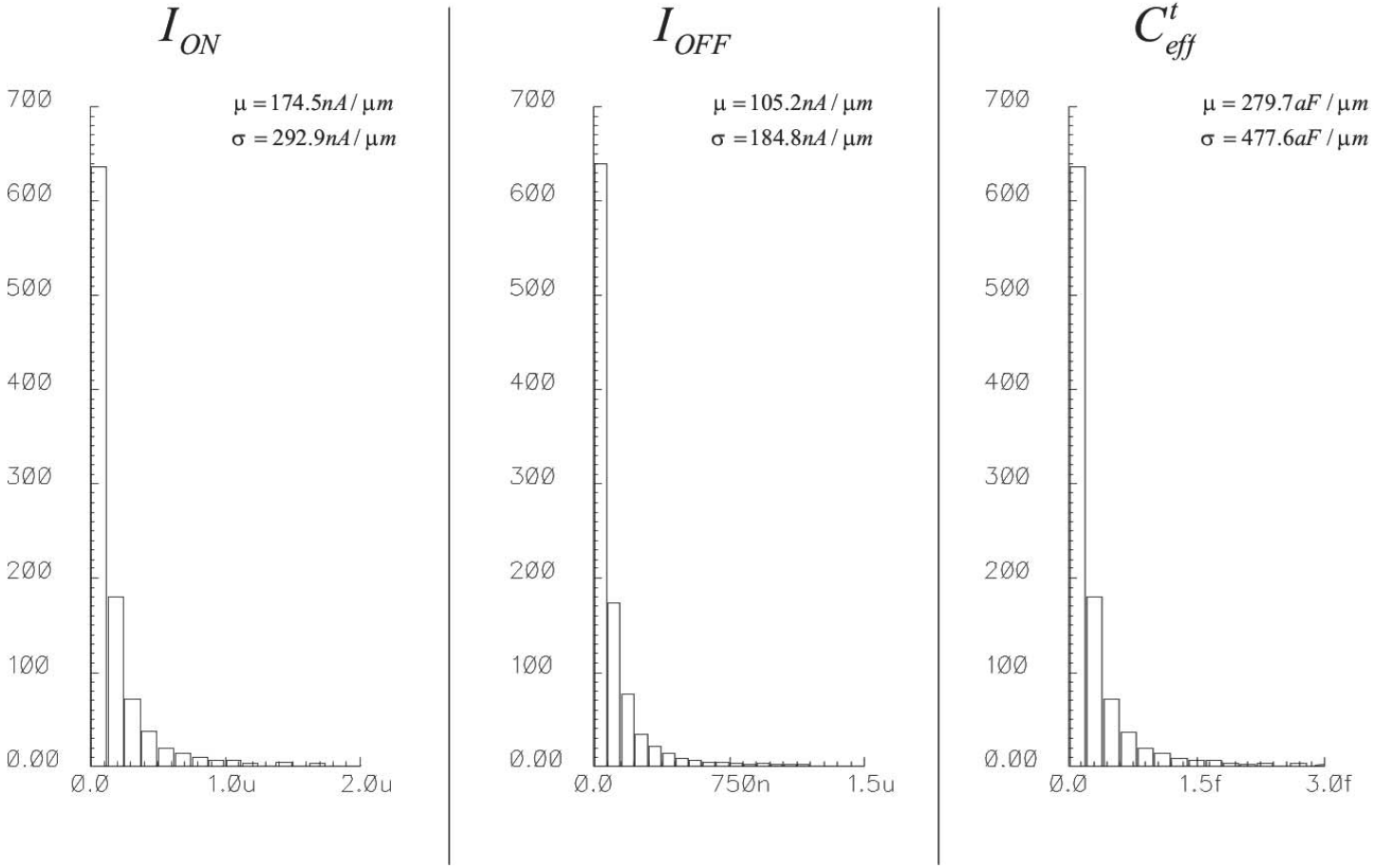


Summary and Conclusions

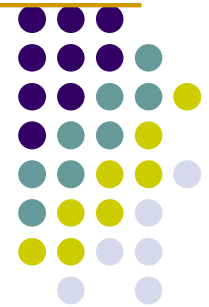
Monte Carlo Simulations: (Modeling Variations)



- Monte Carlo (N=1000) results.
  - 10% variation in gate oxide and supply assumed.

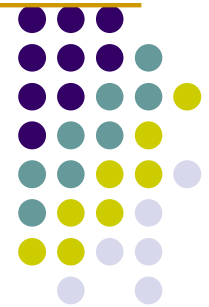


Monte Carlo Simulations: (Modeling Variations)



- All three metrics follow lognormal distribution.
- This is expected since gate T_{ox} and V_{dd} are assumed normally distributed and I_{ox} depends exponentially on both.
- Small parameter variation (10%) leads to large deviance in the metrics (2-3 sigma).

Gate Leakage in Nano-CMOS



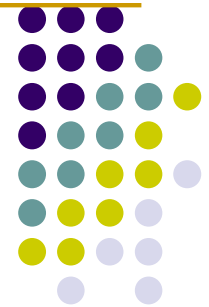
- Both ON and OFF states contribute to gate oxide leakage.
- Transient effect is significant and can be captured via effective tunneling capacitance.
- I_{ON} and I_{OFF} metrics to quantify gate leakage current during steady state.
- C^{eff}_{tun} ≡ Effective tunneling capacitance at the input of a logic gate.

Usefulness of the Proposed Metrics

- The metrics allow designers to account for gate tunneling effect in nano-CMOS based circuit designs.
- I_{ON} and I_{OFF} - additive to static power consumption.
- C^{eff}_{tun} – additive to intrinsic gate capacitance

$$C_{logic} = C^{eff}_{tun} + C_{intrinsic}$$

- All three needs to be taken into account for effective total (switching, subthreshold, gate leakage) power optimization



Thank You

For more information:

http://www.cse.unt.edu/~smohanty