Simultaneous Power Fluctuation and Average Power Minimization during Nano-CMOS Behavioral Synthesis

Saraju P. Mohanty and Elias Kougianos

VLSI Design and CAD Laboratory (VDCL)

University of North Texas, Denton, TX, USA.

Email: smohanty@cse.unt.edu

Outline of the Talk

- CMOS scaling Trends
- Our Contributions and Related Research
- Statistical Power Modelling
- Optimization Approach
- Datapath Component Library
- Experimental Results
- Conclusions

CMOS Scaling Trends

Nano-CMOS Based Systems

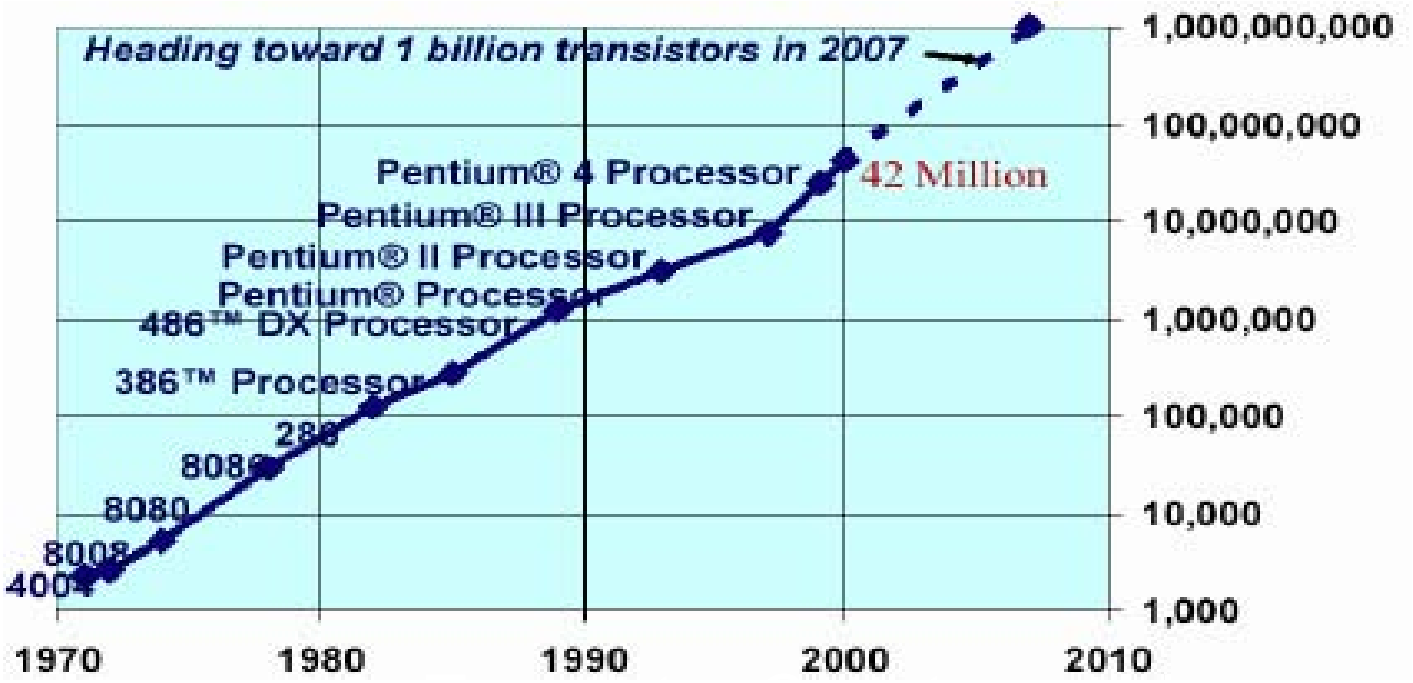
?

Energy costs,
Battery life,
Cooling costs

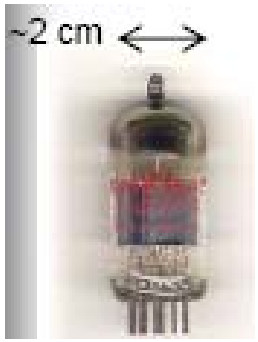
Low Power
Synthesis

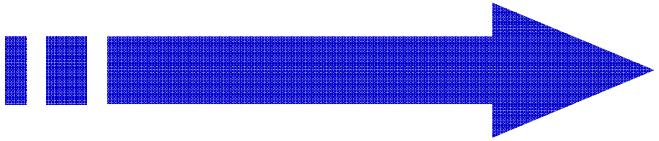
Almost the entire industry today is driven by CMOS.

Scaling Trend – Transistor Count



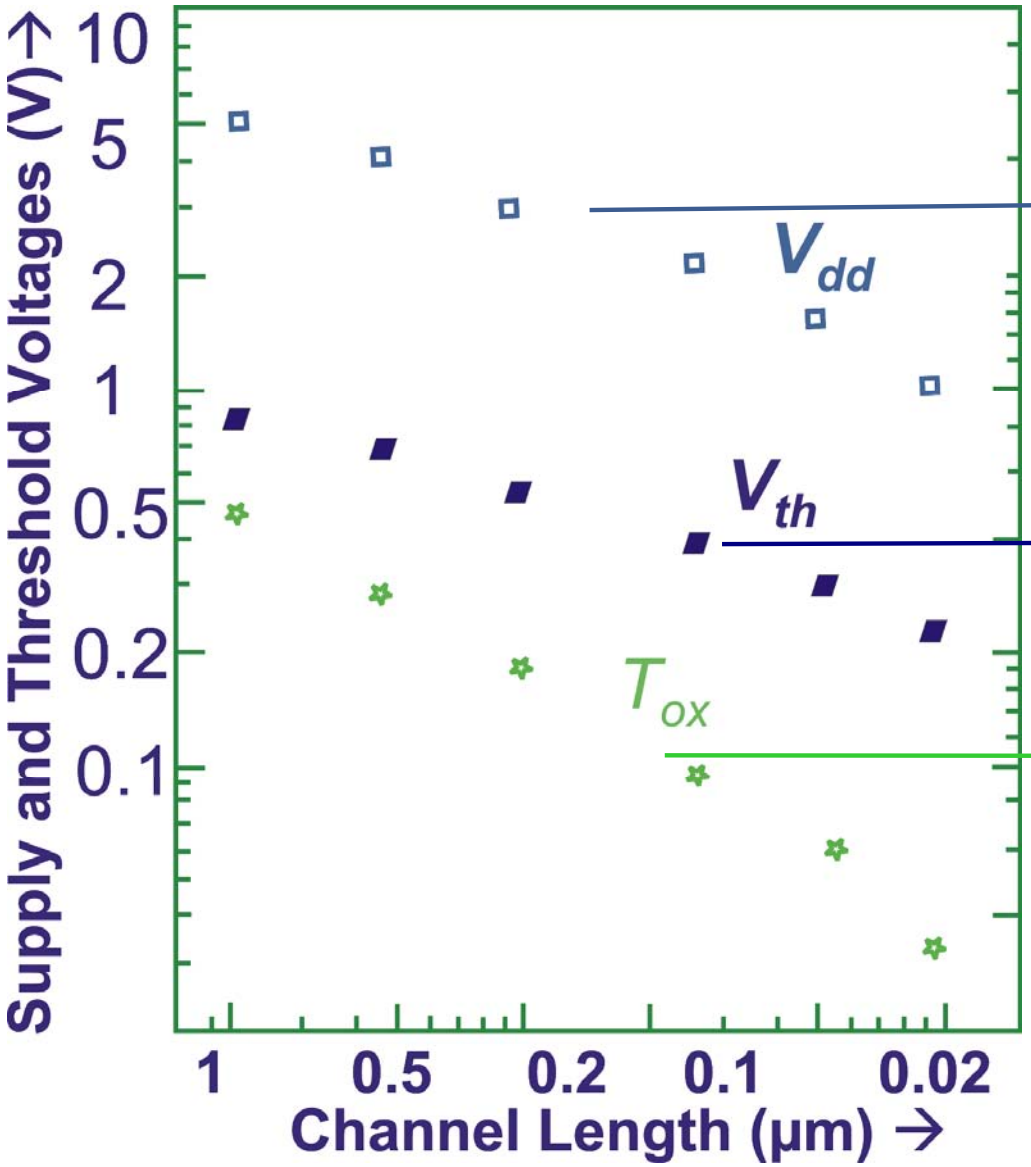
Operating frequency and throughput have increased.





VLSI technology is the fastest growing technology in human history.

What are Scaled ?



Supply Voltage

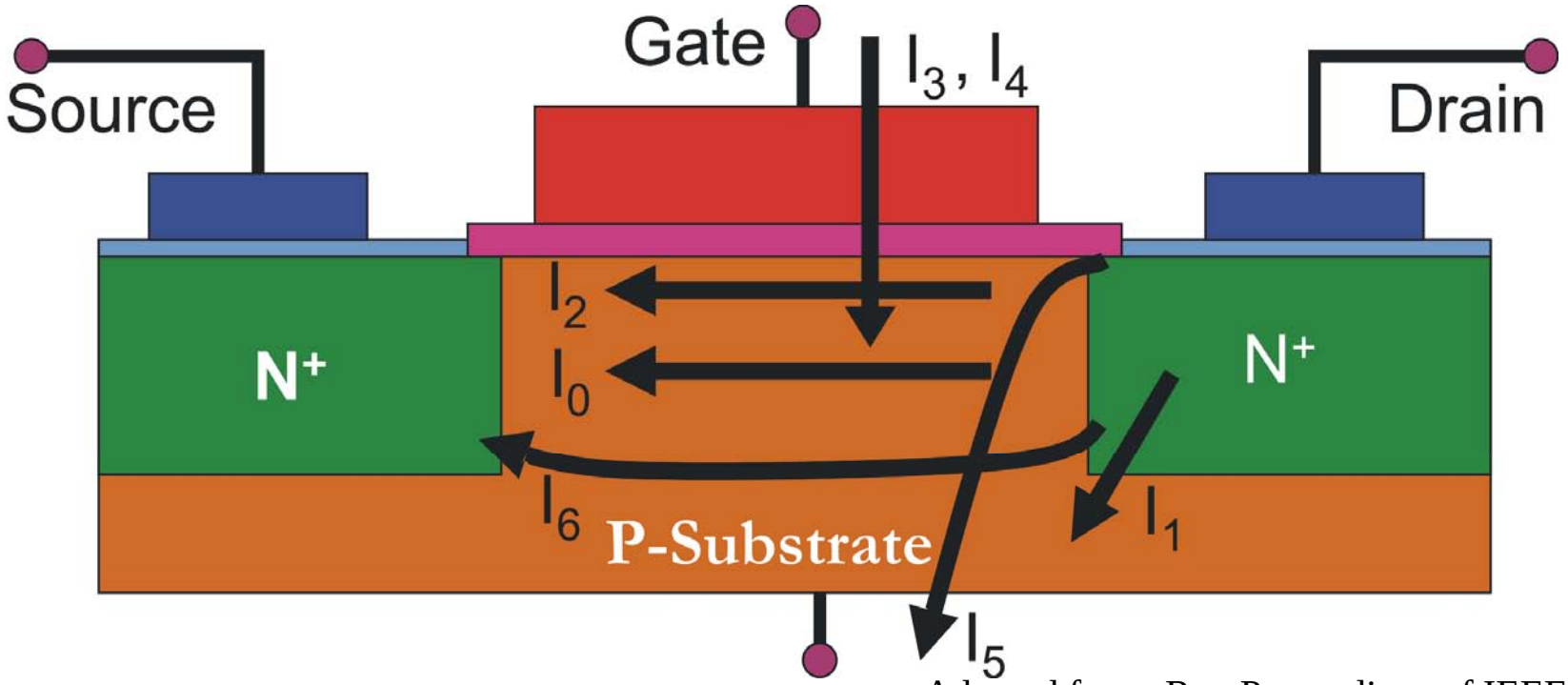
Threshold Voltage

Gate Oxide Thickness

Source: Taur IBM JRD MAR 2002

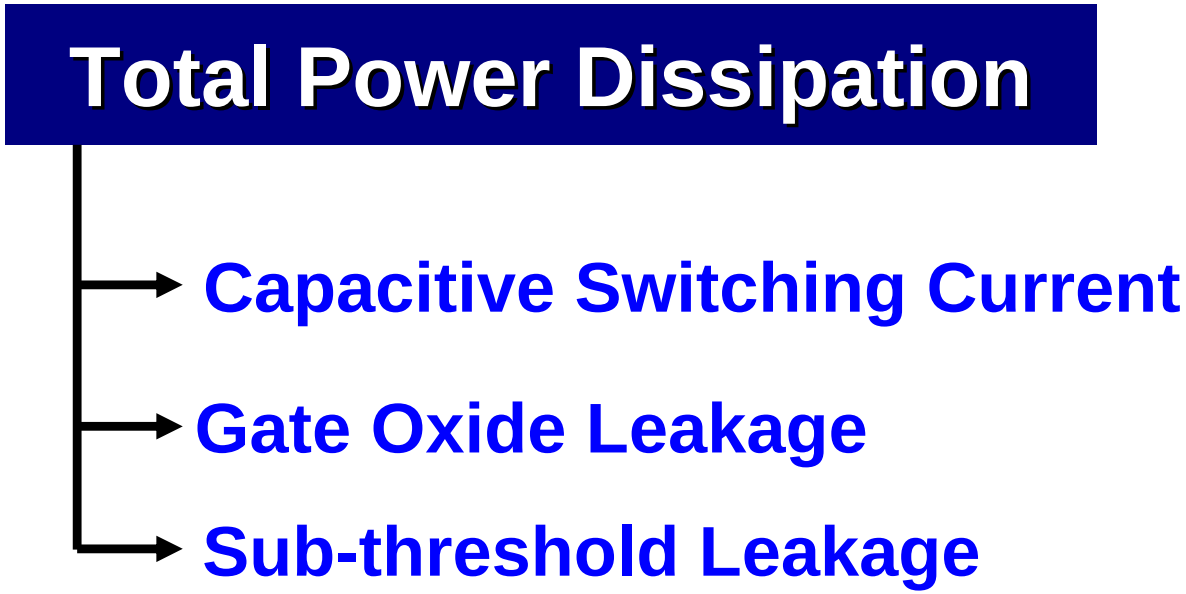
Currents in Nanoscale CMOS

I_0: active drain-to-source current (ON)
I_1: reverse bias pn junction (both ON & OFF)
I_2: subthreshold leakage (OFF)
I_3: oxide tunneling current (both ON & OFF)
I_4: gate current due to hot carrier injection (both ON & OFF)
I_5: gate induced drain leakage (OFF)
I_6: channel punch through current (OFF)



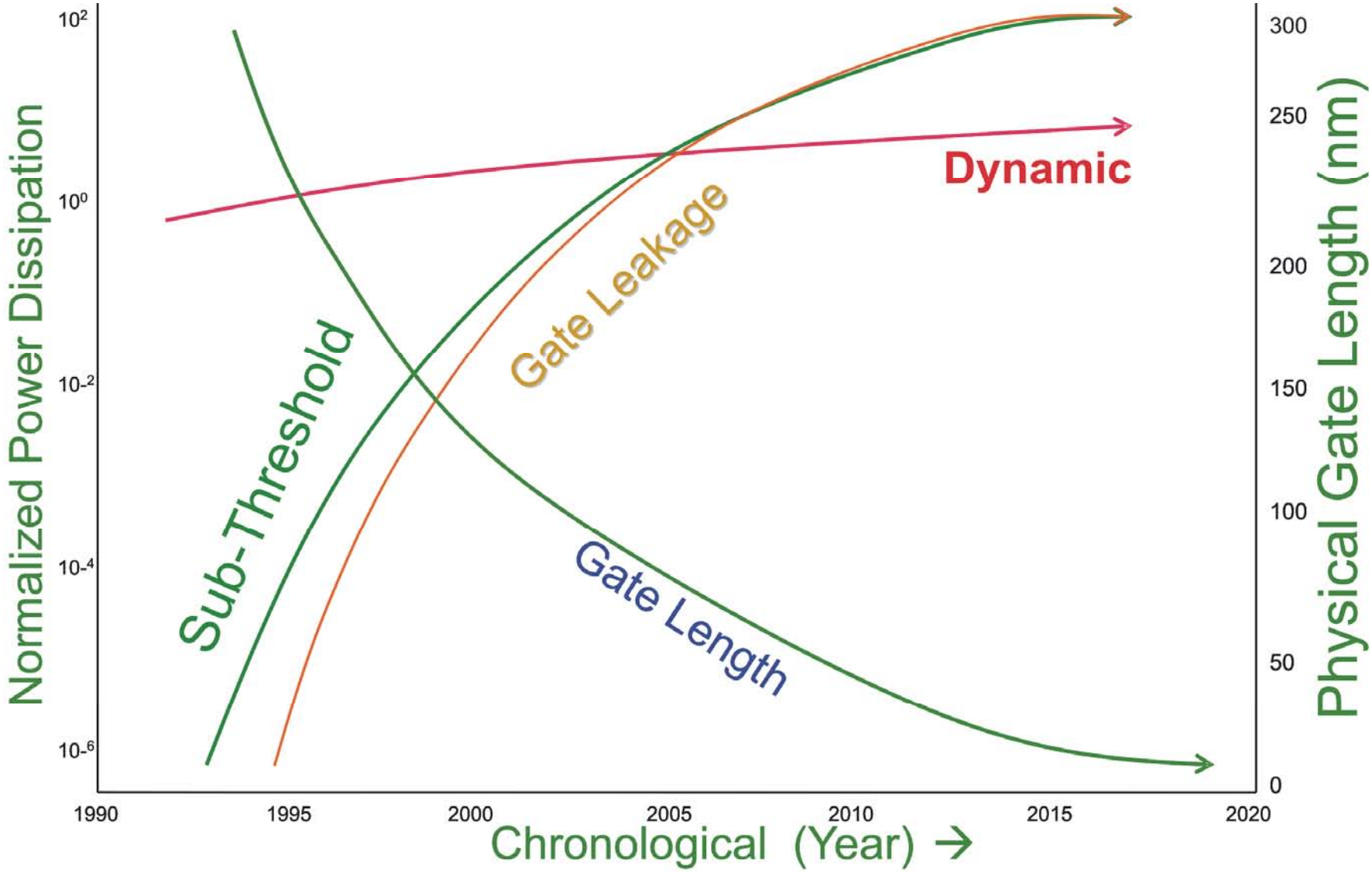
Adopted from: Roy Proceedings of IEEE Feb2003

Power Dissipation in Nano-CMOS: 3 Major Components



The research in this paper intends to simultaneously optimize the three components.

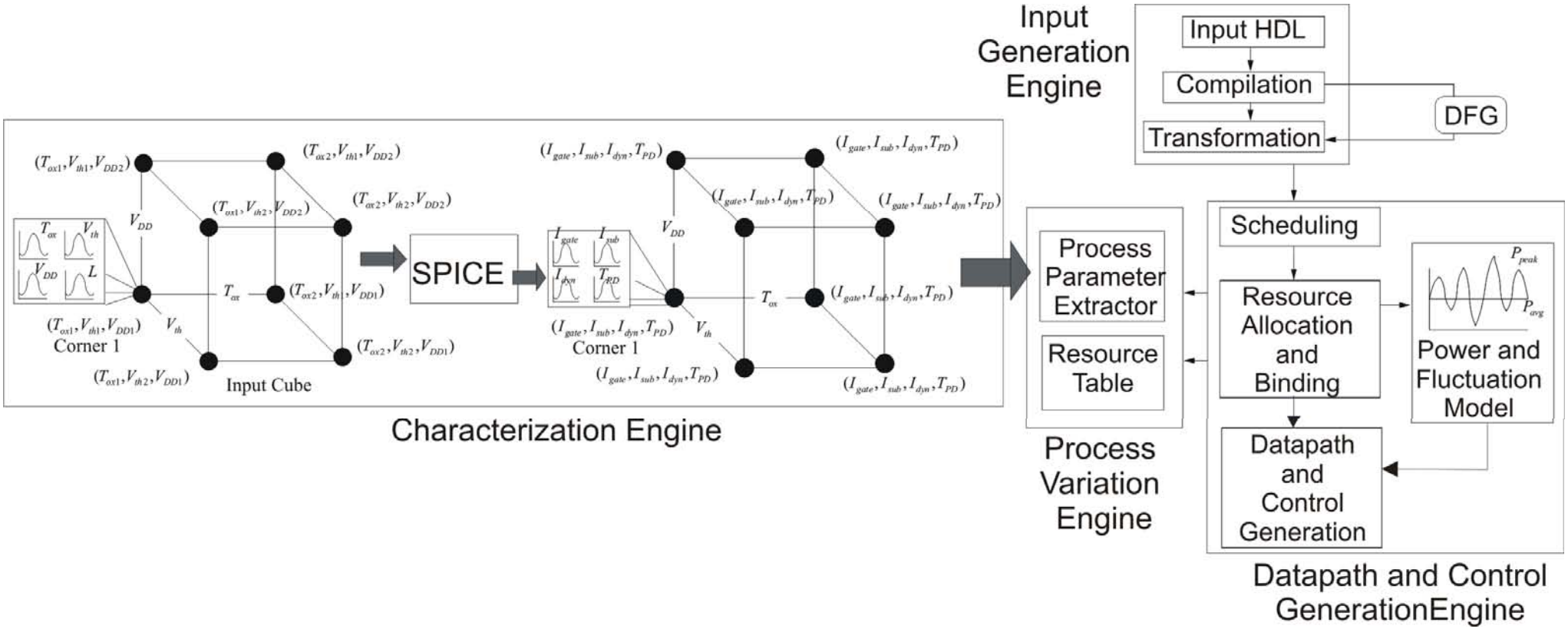
Power Dissipation Trend



Source: Hansen Thesis 2004

Our Contributions and Related Research

Proposed Process Variation Aware High-Level Synthesis



Contributions of Our Paper

- Introduction of an statistical process variation aware datapath component library.
- Introduction of a process variation aware power and fluctuation minimization method.
- Exploration of all design corners of a dual-T_{ox}, dual-V_{th} and dual-V_{DD} technology through Simulated Annealing based optimization algorithm.

Related Research: Dynamic Power

- **Martin, et al. [8]:** Peak dynamic power reduction through scheduling and binding.
- **Mohanty, et al. [11]:** Heuristic method for peak and average dynamic power.
- **Mohanty, et al. [12]:** ILP based method for fluctuation in dynamic power.
- **Raghunathan, et al. [13]:** Simultaneous minimization of peak and peak differential in dynamic power.
- **Shiue [15]:** ILP formulation to reduce peak dynamic power under latency constraints.

Related Research: Leakage Power

- **Gopalakrishnan, et al. [5]:** MTCMOS approach for reduction of subthreshold leakage current.
- **Khouri, et al. [7]:** Algorithms for subthreshold leakage power analysis and reduction using dual threshold voltage.

Related Research: Summary

- Most of the low power high-level synthesis works address average dynamic power reduction.
- Some of them address subthreshold leakage.
- A few address gate oxide leakage.
- Few of them of them address fluctuation in power consumption.
- None of them address the components (dynamic, subthreshold and gate leakage) together.
- None of them account process variation.

Statistical Power Modeling

Overall Objective Function for a Datapath Circuit

Objective function has two parts:

- Average power
- Power fluctuation

$$\chi_{P \cup F}^{Datapath} = \chi_{P}^{DFG} + \chi_{F}^{DFG}$$

Average Power of a Datapath Circuit

Average of power account all forms:

- Switching power
- Gate oxide leakage
- Subthreshold leakage

$$\chi_P^{DFG} = \alpha I_{gate}^{DFG}(\mu,\sigma) + \beta I_{sub}^{DFG}(\mu,\sigma) + \gamma I_{dyn}^{DFG}(\mu,\sigma)$$

Total Fluctuation in Power Consumption of a Datapath Circuit

Total cycle-to-cycle power fluctuation if number of clock cycles (c) is N_{cc}:

$$\chi_F^{DFG} = \sum_{c=1}^{N_{cc}-1} \left| I_{total}^{c}(\mu,\sigma) - I_{total}^{c+1}(\mu,\sigma) \right|$$

Total current in cycles c is:

$$I_{total}^{c}(\mu,\sigma) = I_{gate}^{c}(\mu,\sigma) + I_{sub}^{c}(\mu,\sigma) + I_{dyn}^{c}(\mu,\sigma)$$

Our Optimization Approach During Behavioral Synthesis

Simulated Annealing for Optimization

- Analogous to the annealing process, the mobility of nodes in a DFG is dependent on the total available resources.
- Nodes of a DFG are analogous to the atoms and temperature is analogous to the total number of available resources.
- To minimize the objective function the scheduling and binding need to done using resources from different design corners.

Simulated Annealing Based Optimization

Simulated Annealing Algorithm (UDFG, Constraints, Library)
(01) Perform ASAP and ALAP scheduling.
(02) While there exists a schedule with available resources.
(03) i = Number of iterations
(04) Perform resource constrained ASAP and ALAP
(05) Initial Solution ← ASAP Schedule
(06) S ← Allocate-Bind()
(07) Initial Cost ← Power-Cost(S)
(08) While (i > 0)
(09) Generate random transition from S to S*.
(11) Δ-Cost ← Power-Cost(S) − Power-Cost(S*)
(12) if(Δ-Cost > 0) then S ← S*.
(13) i ← i − 1
(14) end While
(15) Decrement available resources
(16) end While
(17) return S.

Simulated Annealing Based Optimization

Power-Cost (S, Library)

(01) $I_{Totalc} = Current(FU_i(V_{DD}, V_{th}, T_{ox}))$

(02) $PF_c = | I_{Totalc} - I_{Totalc-1} |$

(03) $I_{Total} = \Sigma_c I_{Totalc}$

(04) $PF_{Total} = \Sigma_c PF_c$

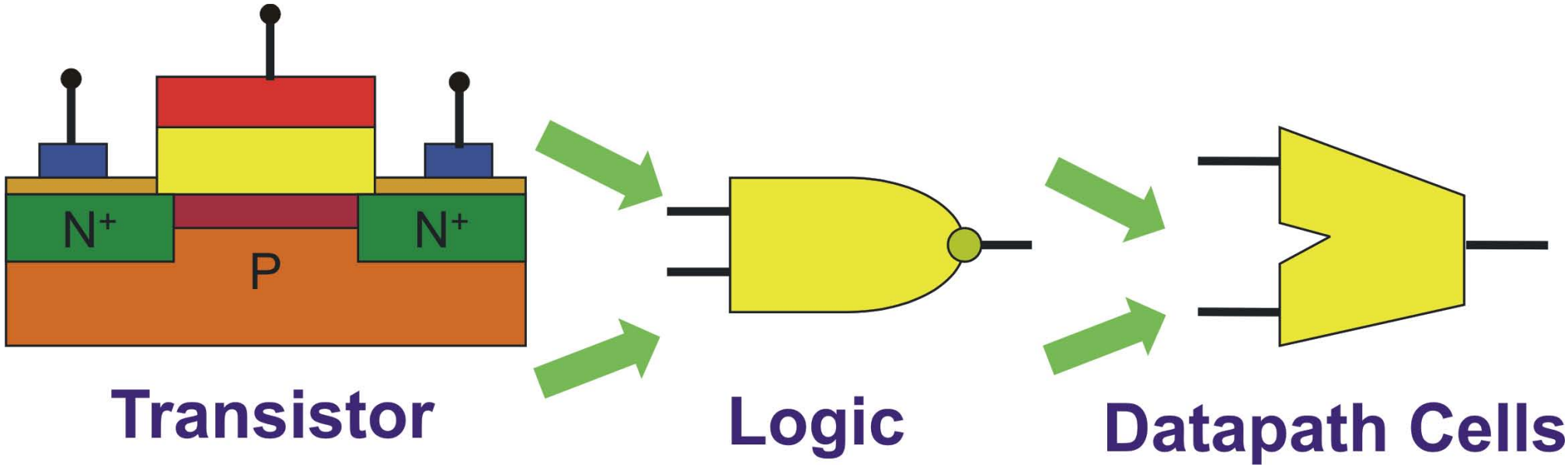
(05) $Cost\text{-}PDF = \theta * I_{Total} + \delta * PF_{Total}$

(06) $Cost = a * \mu(Cost\text{-}PDF) + b * \sigma(Cost\text{-}PDF)$

(07) return Cost.

Process Variation Aware Datapath Component Library

Datapath Component Library: 3-Level Hierarchical Approach

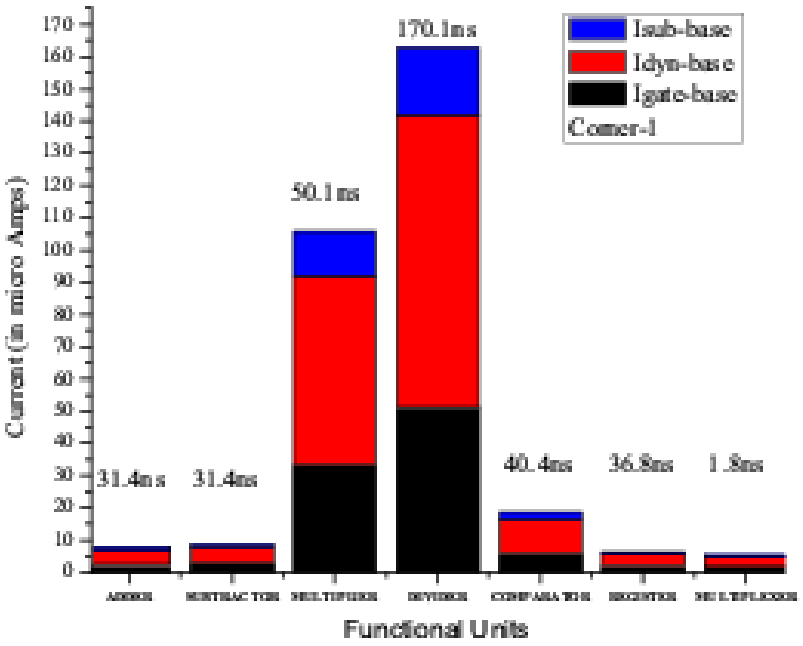


- The BSIM4 deck generated through BPTM represent a hypothetical 45nm CMOS process.
- The nominal values for design corner (1) are: T_{ox} = 1.4nm, V_{th} = 0.22V for NMOS, V_{th} = −0.22V for PMOS, W/L = 4/1 for NMOS, W/L = 8/1 for PMOS, and V_{DD} = 0.7V.

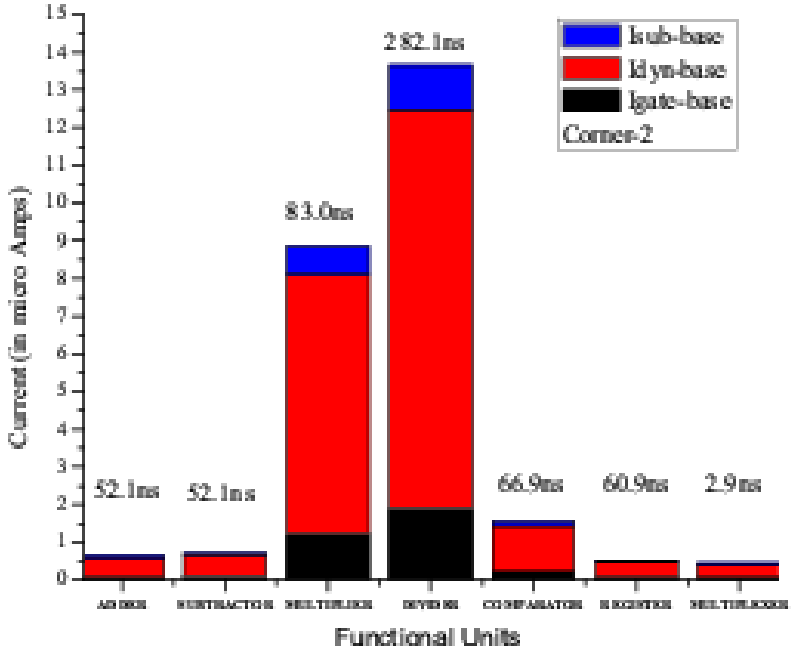
Datapath Component Library

- We assumed that resources such as adders, subtractors, multipliers, dividers, are constructed using 2-input NAND.
- There are total n_{total} NAND gates in the network of NAND gates constituting a *n*-bit functional unit.
- n_{cp} number of NAND gates are in the critical path.
- Through Monte Carlo simulations the input process and design variations are modeled.

Datapath Component Library: Baseline Data

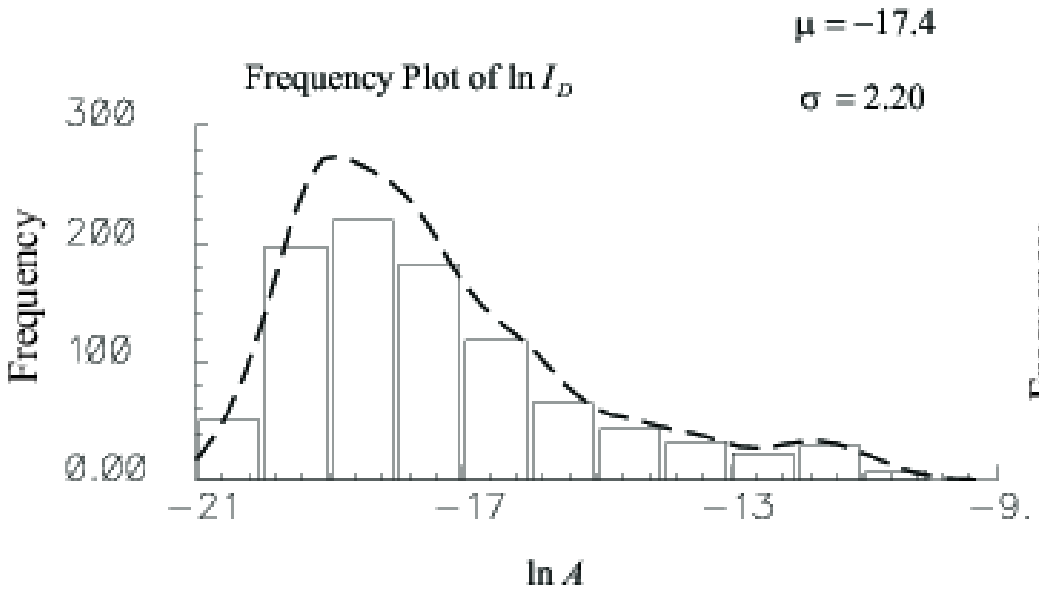


(Corner – 1)

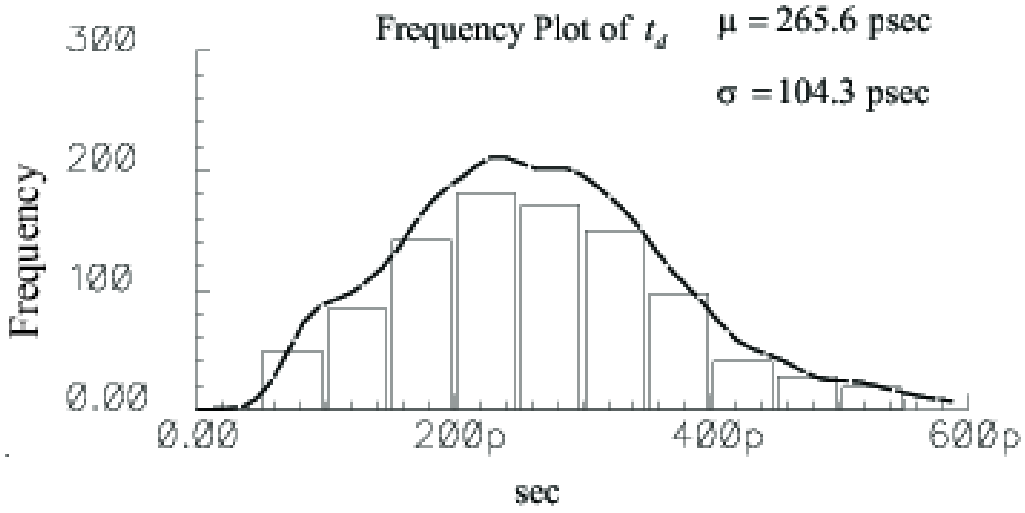


(Corner – 2)

Datapath Component Library: Statistical Data



Dynamic Current



Propagation Delay

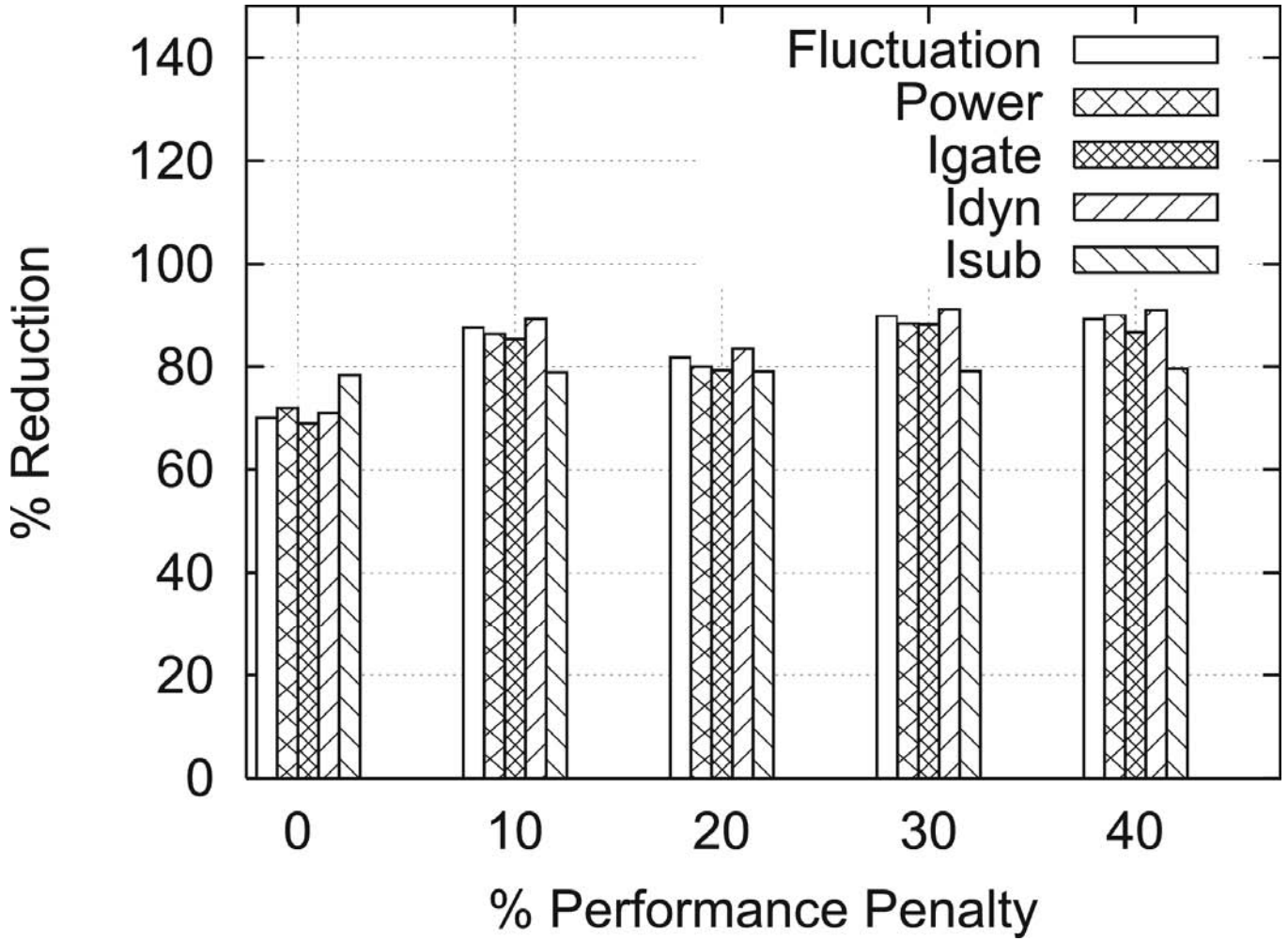
NOTE: Similar results are obtained for gate oxide leakage and subthreshold current.

Experimental Results and Conclusions

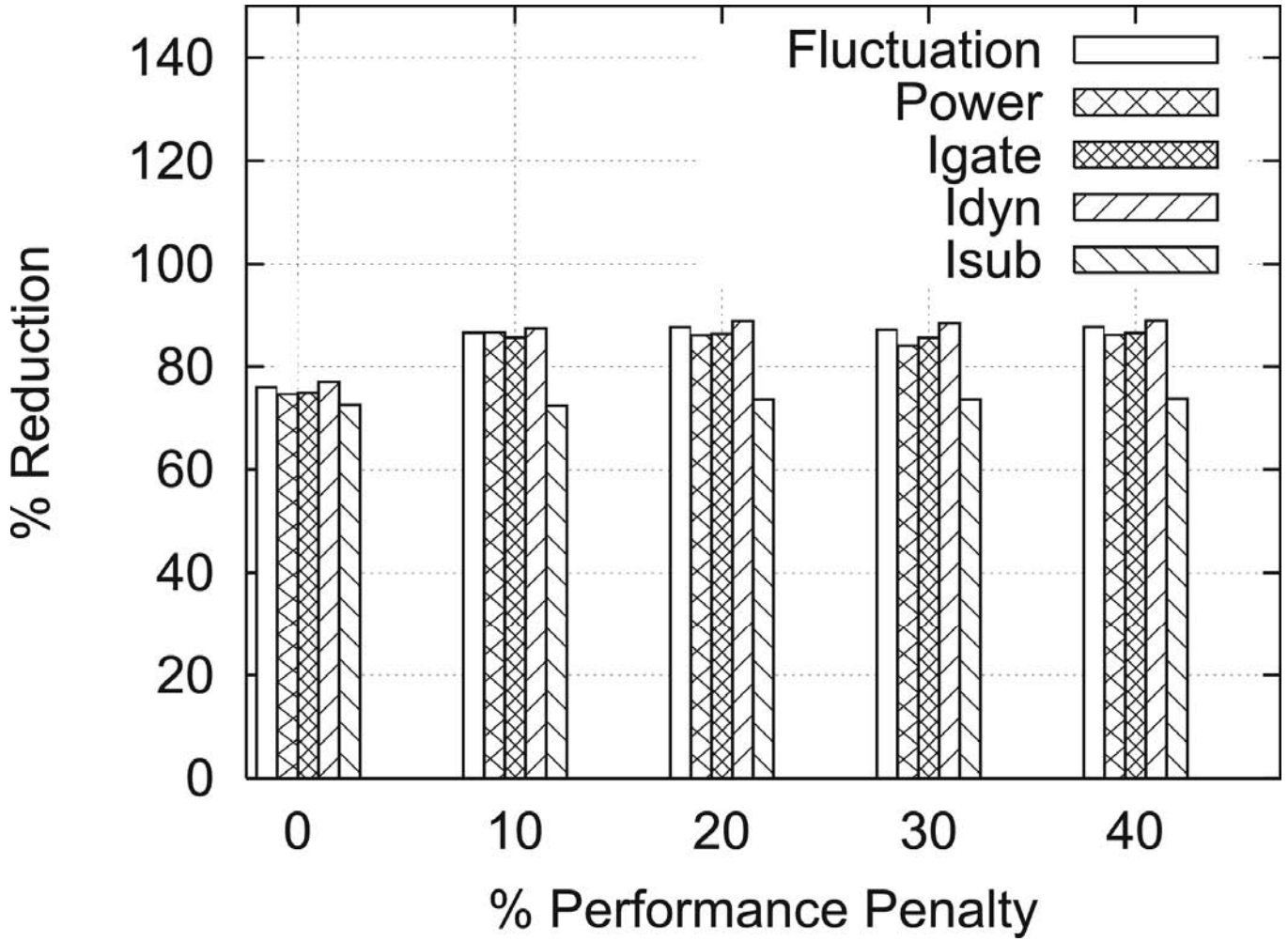
Experimental Results : Setup

- Algorithm implemented in C an integrated in our in-house tool.
- Various different resource constraints are used.
- Time constraints were selected from 1.0 to 1.4 times of the critical path delay.
- Typical simulation time was in the range 20mins to 30 mins.

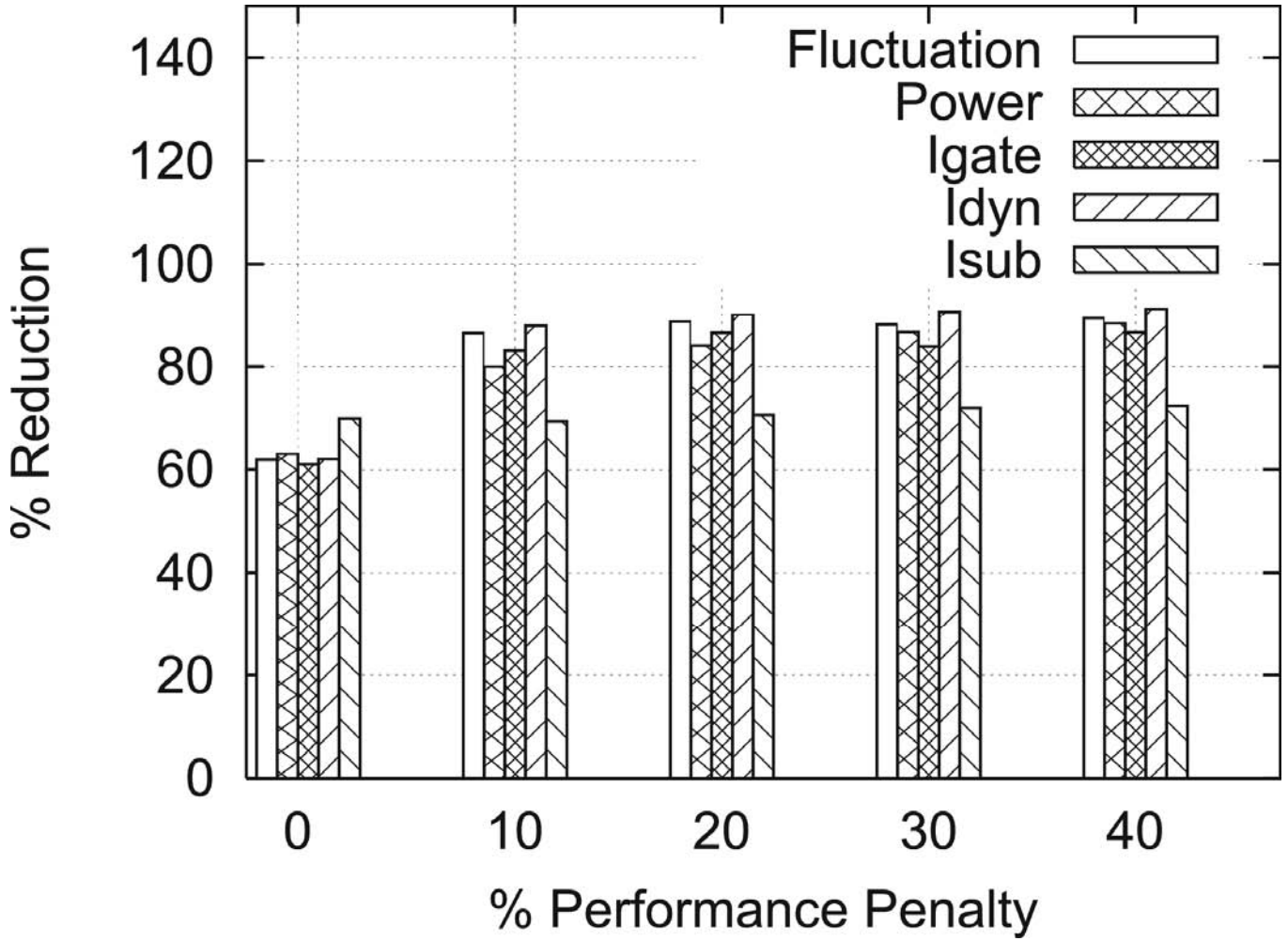
Experimental Results : % Average for DCT



Experimental Results : % Average for FIR



Experimental Results : % Average for HAL



Summary and Conclusions

- Process variation aware power and fluctuation minimization methodology is presented.
- Dual oxide thickness, threshold voltage, and supply voltage technique are used for power reduction.
- Simulated annealing based optimization is used.
- Experimental results showed significant reduction is all forms of power dissipation for all benchmark circuits.

Thank You!