
A Secure Digital Camera (SDC) for Real-Time Security and Copyright Protection of Multimedia

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Outline of the Talk

- Digital Rights Management (DRM)
- Our Proposed Secure Digital Camera (SDC) for real-time DRM
- Our Low-Power Watermarking Chip for the SDC
- Research Challenges for Security, Power (Battery), and Performance Tradeoffs
- Application Scenarios for the SDC

Digital Rights Management (DRM)

Mobile Electronic Appliances



Mobile Phone



PDA



Digital Camera

What is common ??



Video Phone



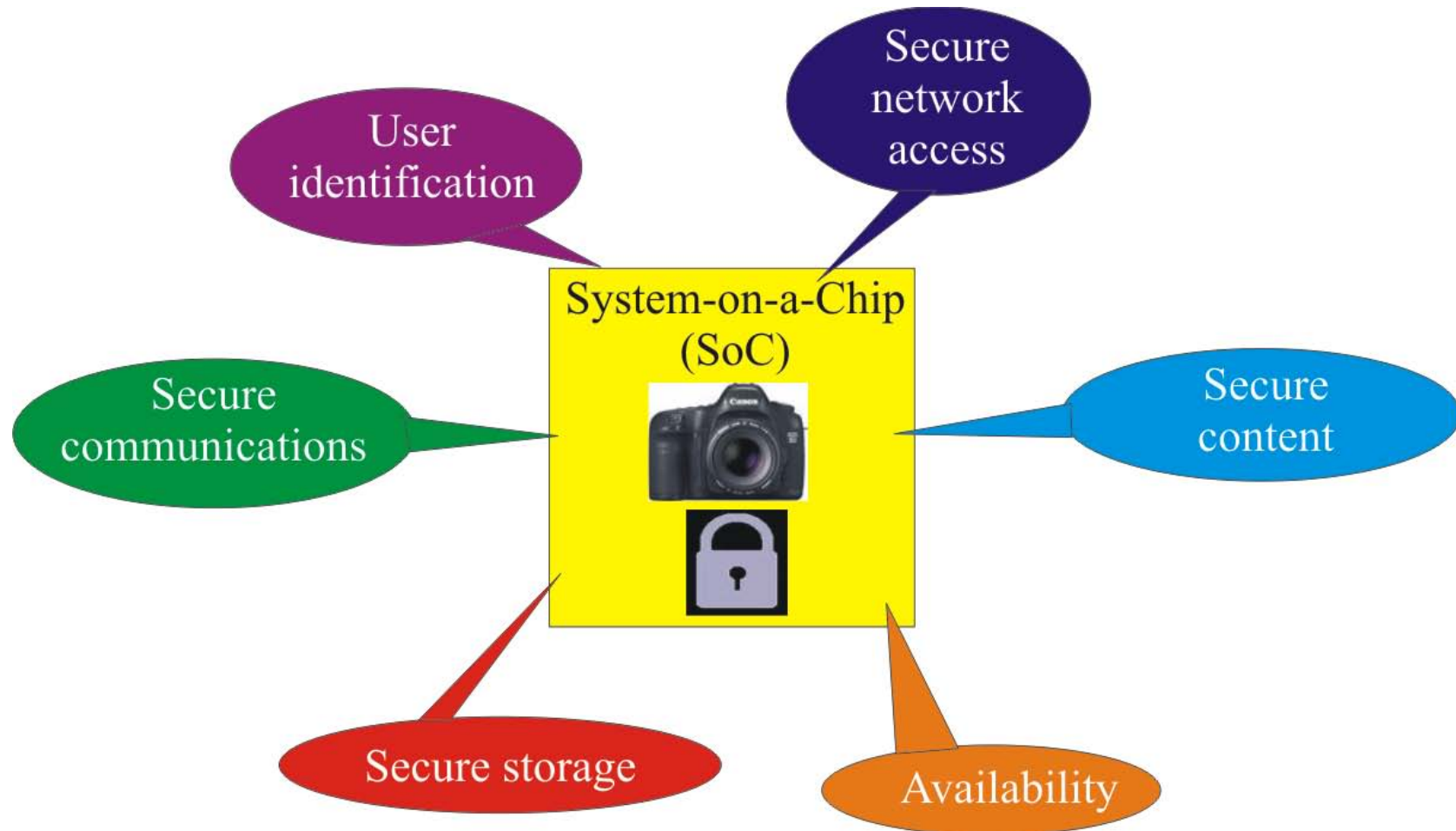
Router



Digital Camcorder

- They access, store, and process multimedia data.
- They are embedded systems designed as System-on-Chips (SoCs).
- They consume power (energy).

Security Requirements in SoCs : Big Picture



- Content security is of our interest which will be handled through digital rights management (DRM) facility.

DRM : Definition

- Digital Rights Management (DRM) is a generic term that refers to any of several technologies used by publishers, creators, or owners to control (restrict) access and usage of digital data.
- Typically a DRM system:
 - Protects intellectual property by either encrypting the data so that it can only be accessed by authorized users.
 - and/or
 - Marks the content with a digital watermark, so that the content can not be freely distributed.

DRM : Objectives



- Whose is it?
- Is it tampered with?
- Where was it created?
- Who had created it?
- ... and more.



DRM : Associated Techniques

- Watermarking / Steganography: Embed additional data into a multimedia object visibly or invisibly.
- Cryptography / Scrambling / Hashing: Transform multimedia data from plain form to another form using various functions.
- Digital Certificates: Link between the person and his virtual identity through a cryptographic key.
- Fingerprinting: Marks each copy with the purchaser's information using watermarking such that if the purchaser makes illegitimate copies, they will contain his information.
- and more ...

DRM : Examples

Watermarking



Cryptography



Our Solution for DRM: Secure Digital Camera (SDC)

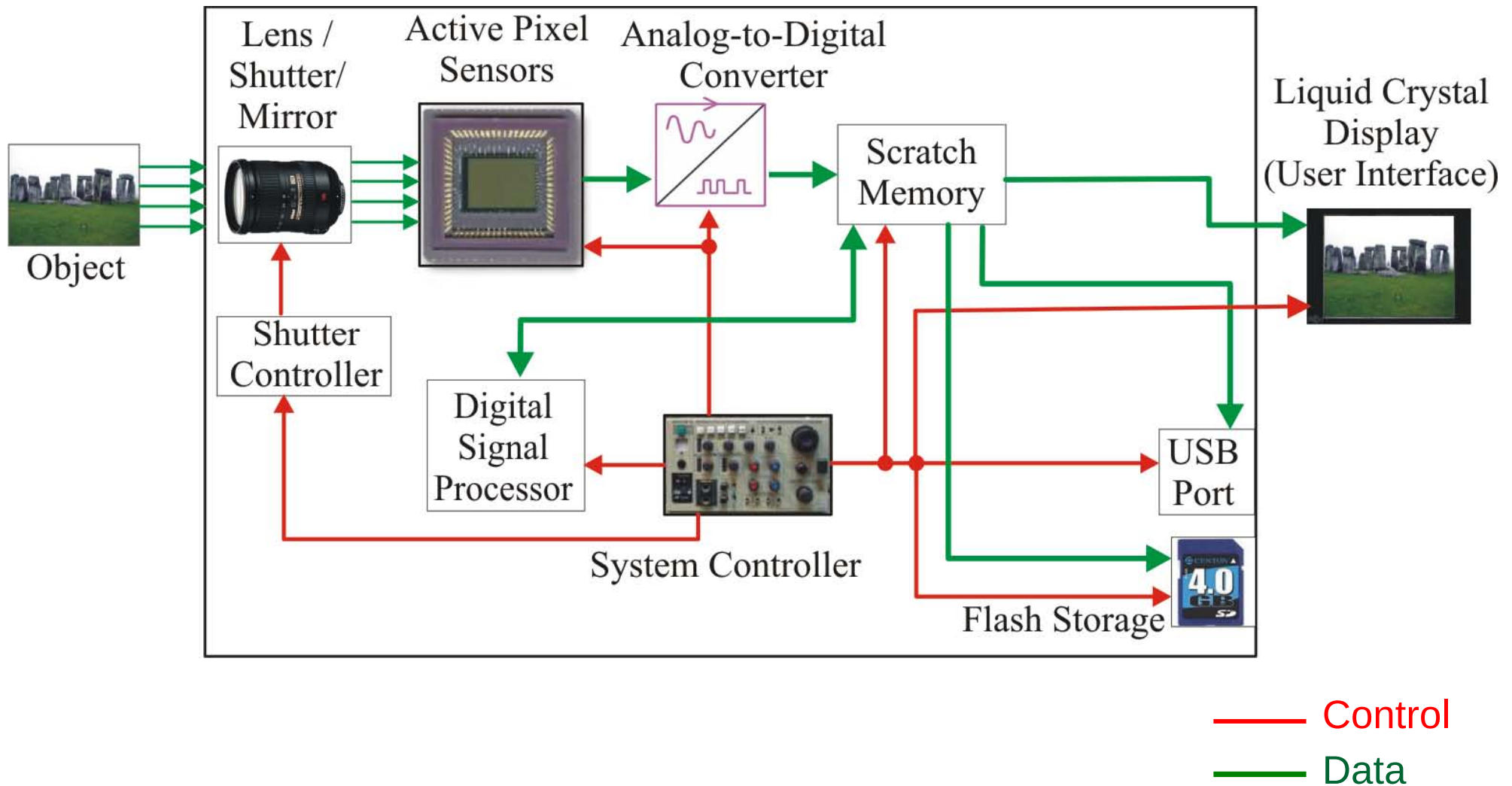
Secure Digital Camera

- An apparatus (system-on-a-chip, SoC) with standards features of digital camera and built in facility for real-time, low-cost, low-power DRM.
- For a given image/video SDC needs to prove:
 - Copyright (visible watermarking)
 - Extent of tampering (invisible-fragile watermarking)
 - Source of image i.e. camera information, place, or date (invisible-robust or visible watermarking)
 - Owner's, Creator's, or Cameraman's information (invisible-robust or visible watermarking)
 - and more.

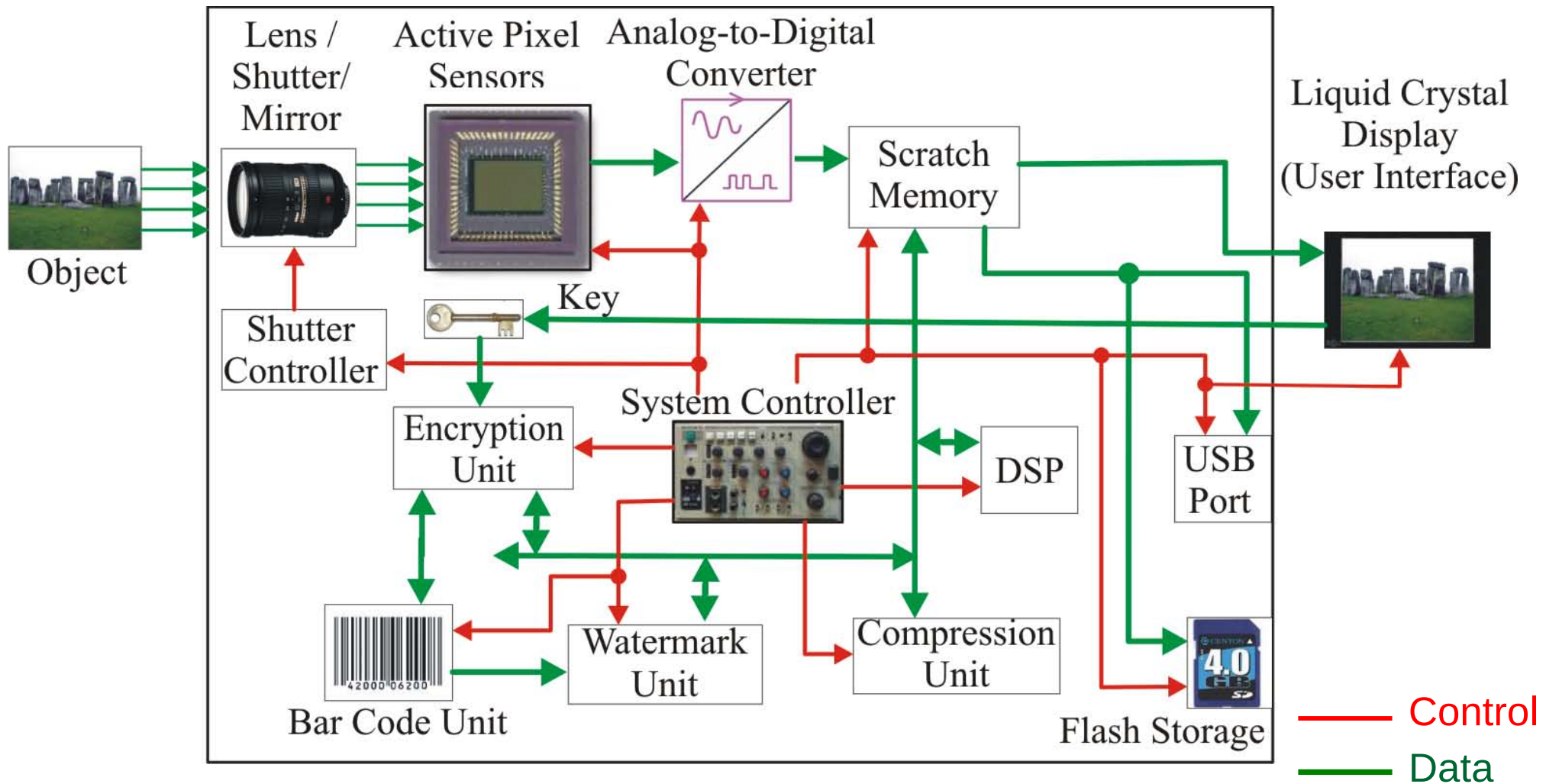
Digital Camera: Internals



Digital Camera: Typical System



Proposed Secure Digital Camera (System-on-a-Chip: SoC)



Hardware Based DRM: Advantages

- Easy integration with multimedia hardware, such as digital camera, camcorder, etc.
- Low-power consumption compared to software.
- High-performance compared to software.
- Higher reliability and availability compared to software.
- More useful for real-time applications like digital video broadcasting.
- Low-cost compared to having explicit software.

Existing Digital Cameras with Watermarking Capability

Epson PhotoPC 3000Z:

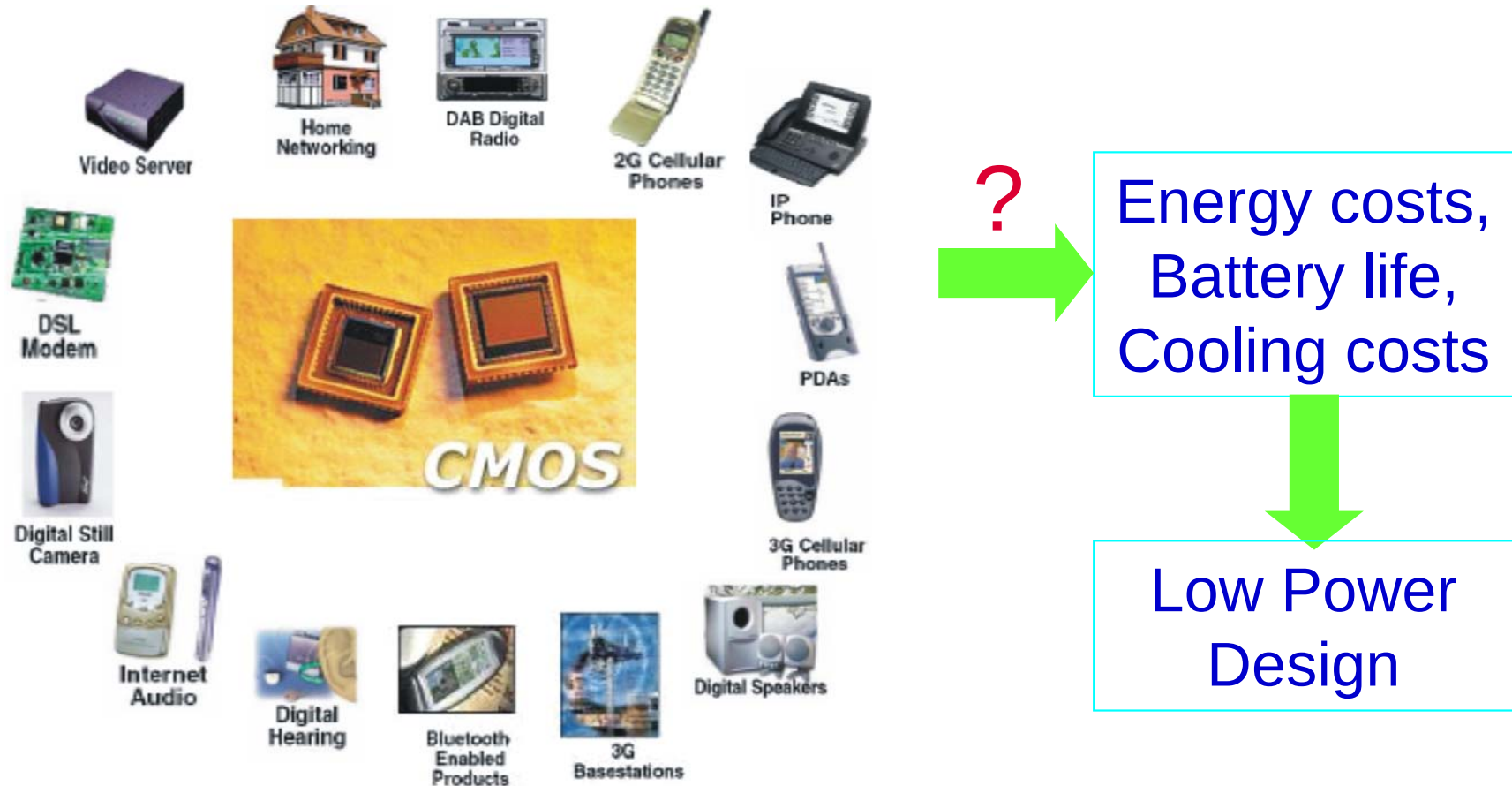
- ❑ Watermark is invisible.
- ❑ Requires optional watermarking offline software for embedding and viewing of watermark.

Kodak DC-290:

- ❑ Visible watermarking only.
- ❑ Watermarking capabilities built into camera.
- ❑ Watermark logo can be added after picture is taken.

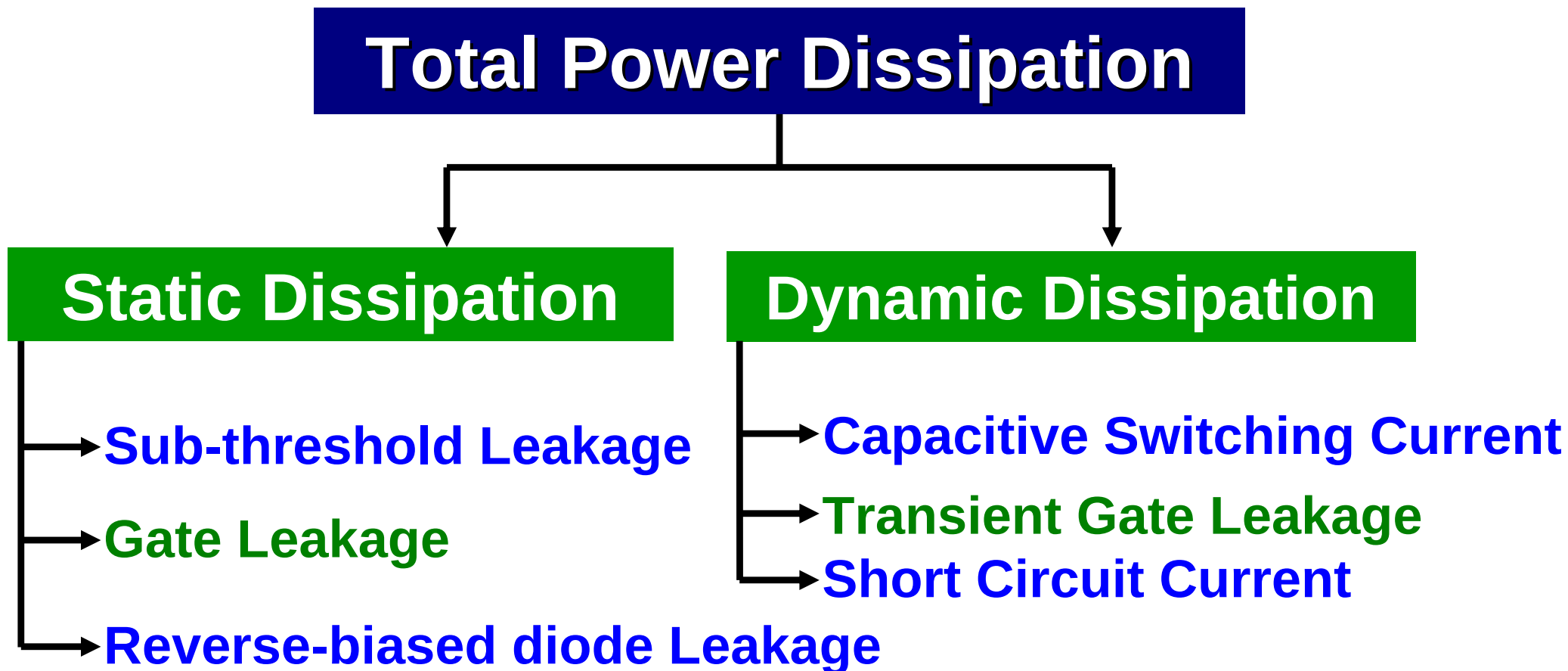
A Visible-Transparent / Invisible-Robust Watermarking Low-Power Chip

Nano-CMOS Based Systems



Almost the entire electronic appliance industry today is driven by nano-CMOS technology.

Power Dissipation in Nano-CMOS Based Systems



Our Low-Power Design Approach

Adjust the frequency and supply voltage in a co-coordinated manner to reduce dynamic power while maintaining performance.

Highlights of our Proposed Chip

- DCT domain implementation.
- First to insert both visible and / or invisible watermark.
- First low-power design for watermarking using dual voltage and dual frequency.
- Uses pipelined and parallelization for better performance.
- Decentralized controller scheme indirectly implements clock gating for power reduction.

Algorithms Selected for the Chip

■ Visible watermarking algorithm:

S. P. Mohanty, K. R. Ramakrishnan and M. S. Kankanhalli, "A DCT Domain Visible Watermarking Technique for Images", in *Proceedings of the IEEE International Conference on Multimedia and Expo*, 2000, pp. 1029-1032.

■ Invisible watermarking algorithm:

I. J. Cox, J. Kilian, T. Leighton, T. Shamoon, "Secure Spread Spectrum Watermarking for Multimedia", *IEEE Transactions on Image Processing*, Vol. 6, No. 12, 1997, pp. 1673-1687.

NOTE: Highest cited papers in respective category.

Invisible Watermarking Algorithm: Original Version

- DCT of the entire original image is computed assuming it as one block.
- The perceptually significant regions of the image are found out. The authors have used 1000 largest coefficients.
- The watermark $X = \{x_1, x_2, \dots, x_n\}$ is computed where each x_i is chosen according to $N(0, 1)$, where $N(0, 1)$ denotes a normal distribution with mean 0 and variance 1.
- The watermark is inserted in the DCT domain of the image by setting the frequency components v_i in the original image to v_i^* using the following for scalar factor α :

$$v_i^* = v_i (1 + \alpha x_i)$$

Invisible Watermarking Algorithm: Modified Version

1. Divide the original image into blocks.
2. Calculate the DCT coefficients of all the image blocks.
3. Generate random numbers to use as watermark.
4. Consider the 3 largest AC-DCT coefficients of an image block for watermark insertion.

Visible Watermarking Algorithm

1. Divide original and watermark image into blocks.
2. Calculate DCT coefficients of all the blocks.
3. Find the edge blocks in the original image.
4. Find the local and global statistics (μ , σ) of original image using DC-DCT and AC-DCT coefficients.
5. Calculate the scaling and embedding factors.
6. Add the original image DCT coefficients and the watermark DCT coefficients block by block.

Visible Watermarking Algorithm

- The α_k and β_k for edge blocks are taken to be $\alpha_{\max}$ and $\beta_{\min}$, respectively.
- For non-edge blocks α_k and β_k are computed as:

$$\alpha_k = \sigma_{AC_{Ik}}^* \left[\exp \left\{ - (\mu_{DC_{Ik}}^* - \mu_{DC_I}^*)^2 \right\} \right]$$
$$\beta_k = \frac{1}{\sigma_{AC_{Ik}}^*} \left[1 - \exp \left\{ - (\mu_{DC_{Ik}}^* - \mu_{DC_I}^*)^2 \right\} \right]$$

- α_k and β_k are then scaled to the ranges $(\alpha_{\min}, \alpha_{\max})$ and $(\beta_{\min}, \beta_{\max})$, respectively.

Visible Watermarking Algorithm: Modifications

- Use $c_{lwhite}(0,0)$ for normalization instead of $c_{lmax}(0,0)$.

- Rewrite α_k and β_k equations:

$$\alpha_k = \frac{\sigma_{AC_{lk}}}{\sigma_{AC_{lmax}}} \left[\exp \left\{ - (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^2 \right\} \right]$$

$$\beta_k = \frac{\sigma_{AC_{lmax}}}{\sigma_{AC_{lk}}} \left[1 - \exp \left\{ - (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^2 \right\} \right]$$

- Remove $\sigma_{AC_{lmax}}$:

$$\alpha^c_k = \sigma_{AC_{lk}} \left[\exp \left\{ - (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^2 \right\} \right]$$

$$\beta^c_k = \frac{1}{\sigma_{AC_{lk}}} \left[1 - \exp \left\{ - (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^2 \right\} \right]$$

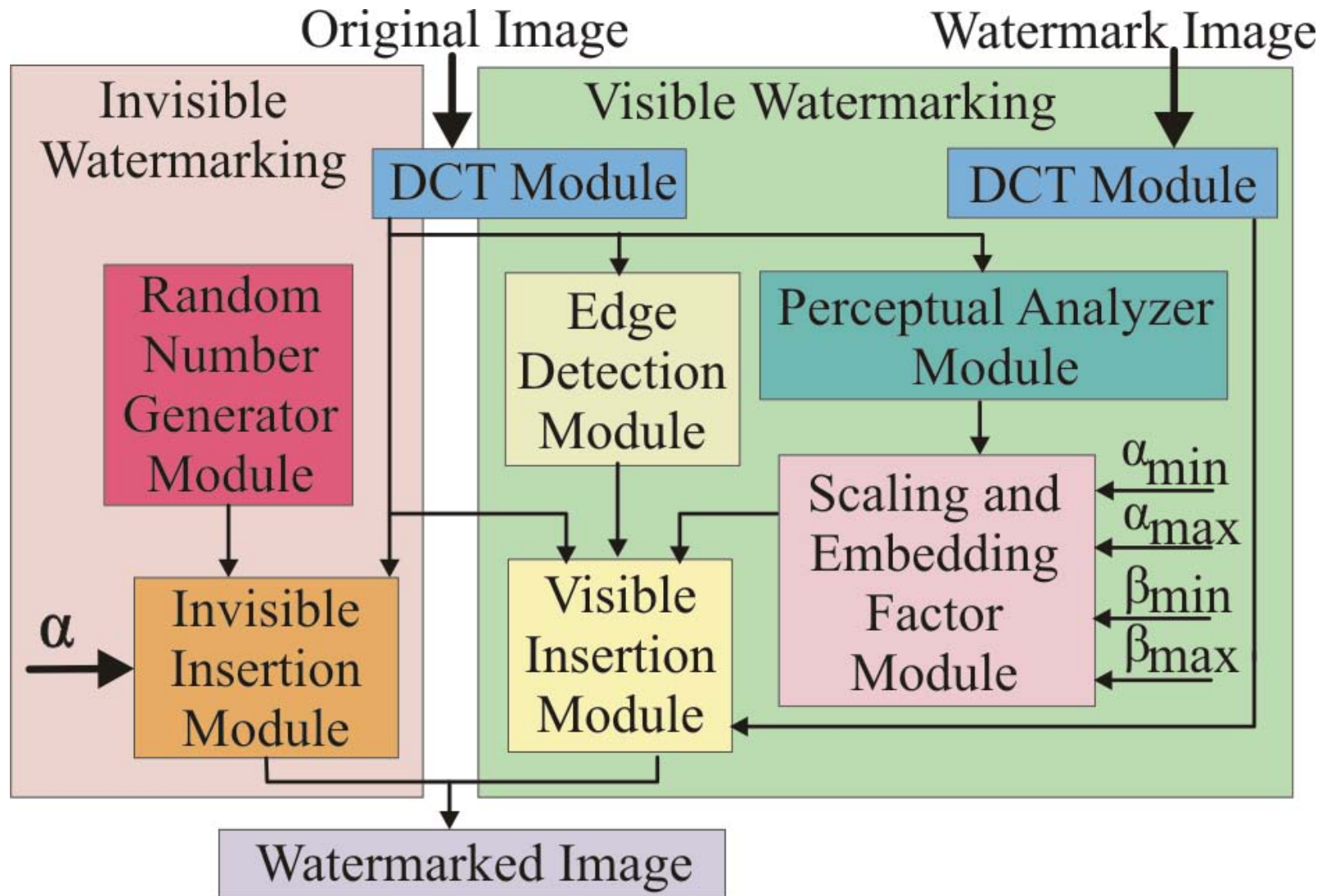
- Remove exponential using Taylor series:

$$\alpha^c_k = \sigma_{AC_{lk}} \left\{ 1 - (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^2 + (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^4 \right\}$$

$$\beta^c_k = \frac{1}{\sigma_{AC_{lk}}} \left\{ (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^2 - (\mu_{DC_{lk}}^* - \mu_{DC_I}^*)^4 \right\}$$

- Scale to the ranges $(\alpha_{min}, \alpha_{max})$ and $(\beta_{min}, \beta_{max})$, respectively.

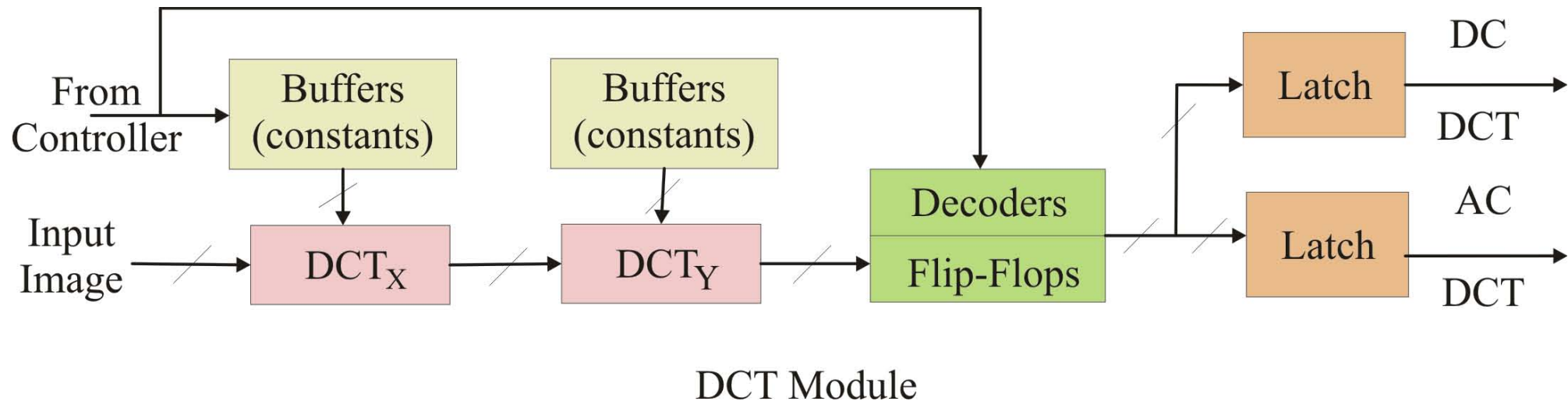
The Proposed Architecture



The Proposed Architecture: Modules

- **DCT Module:** Calculates the DCT coefficients.
- **Edge Detection Module:** Determines edge blocks.
- **Perceptual Analyzer Module:** Determines perceptually significant regions using original image statistics.
- **Scaling and Embedding Factor Module:** Determines the scaling and embedding factors for visible watermark insertion.
- **Watermark Insertion Module:** Inserts the watermark.
- **Random Number Generator Module:** Generates random numbers.

The Proposed Architecture (DCT Module)



- Computes DCT of a 4x4 block.
- Both DCTX and DCTY modules have similar architectures.

The Proposed Architecture (DCT Module)

DCT module implements the following equations:

$$x_{00} = ((in_{00} * c_{00}) + (in_{01} * c_{01}) + (in_{02} * c_{02}) + (in_{03} * c_{03}))$$

$$x_{10} = ((in_{10} * c_{00}) + (in_{11} * c_{01}) + (in_{12} * c_{02}) + (in_{13} * c_{03}))$$

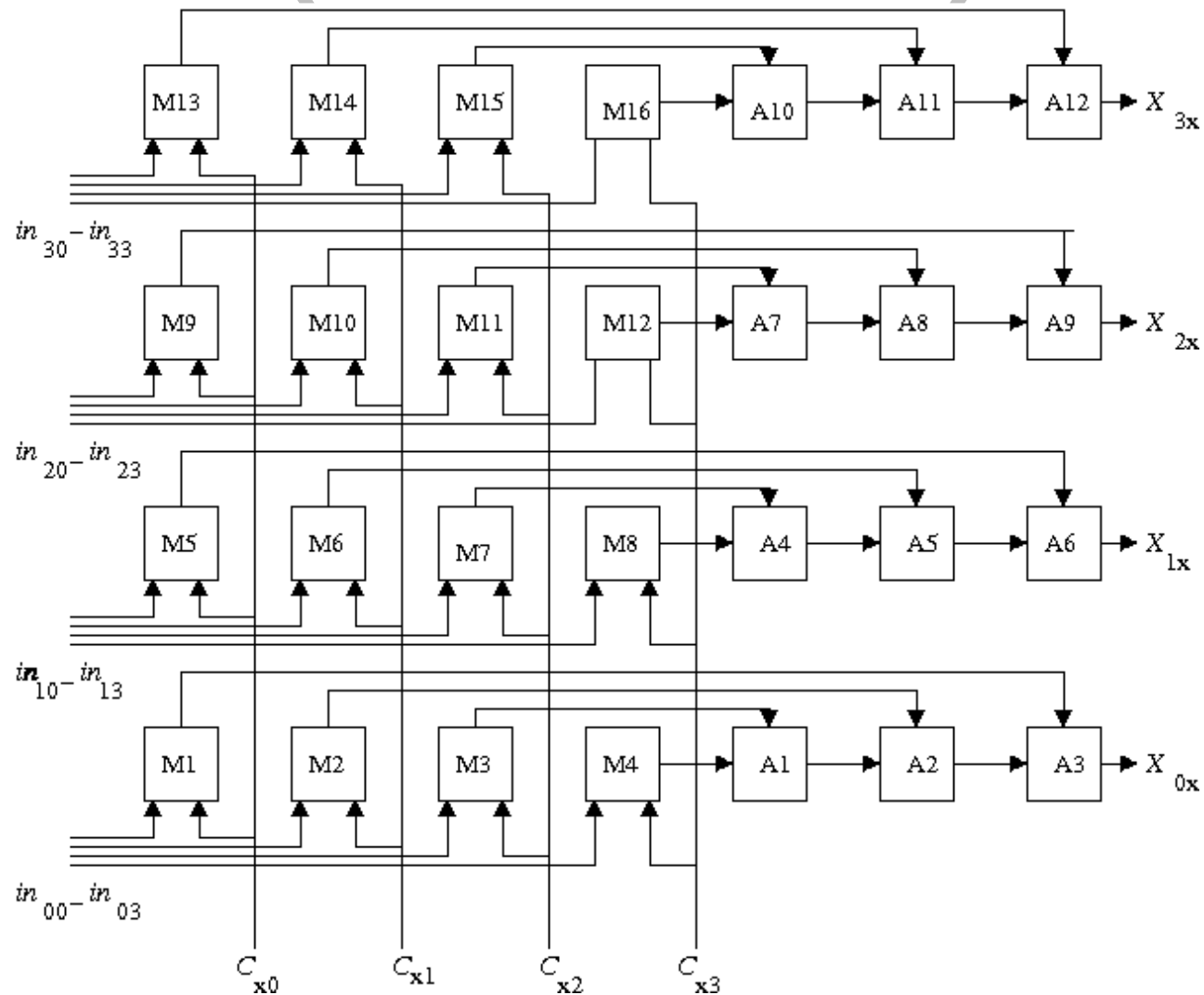
$$x_{20} = ((in_{20} * c_{00}) + (in_{21} * c_{01}) + (in_{22} * c_{02}) + (in_{23} * c_{03}))$$

$$x_{30} = ((in_{30} * c_{00}) + (in_{31} * c_{01}) + (in_{32} * c_{02}) + (in_{33} * c_{03}))$$

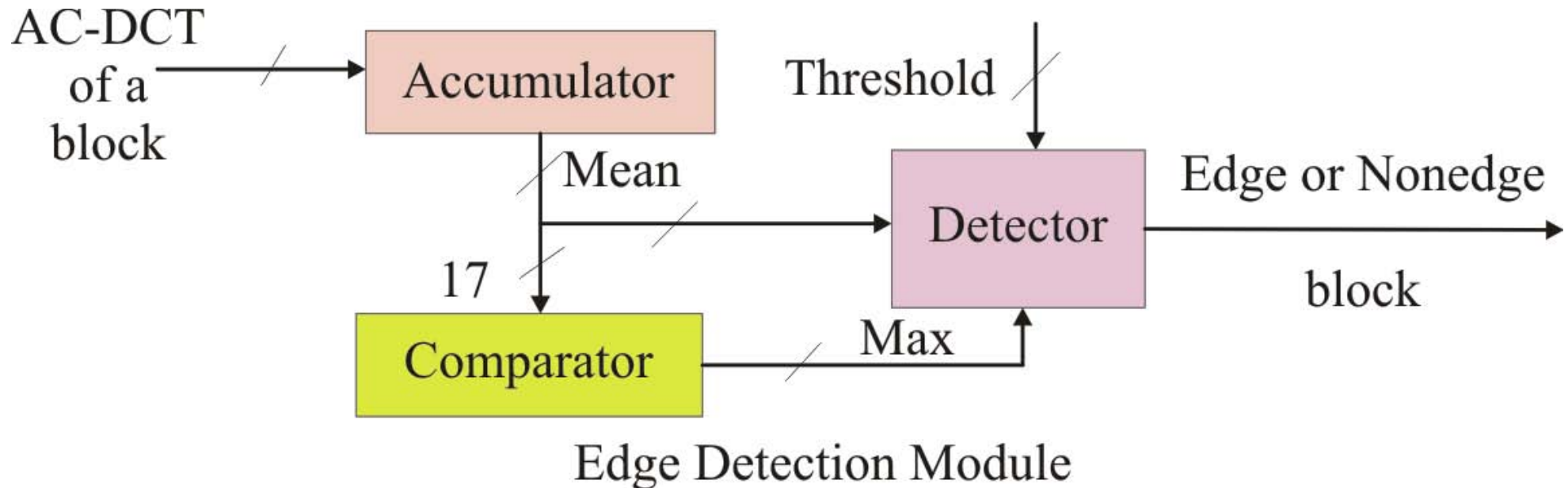
NOTE:

- in_{ij} – input, c_{ij} – constants, x_{ij} – coefficients
- 16 multiplications and 12 additions involved

The Proposed Architecture (DCT Module)

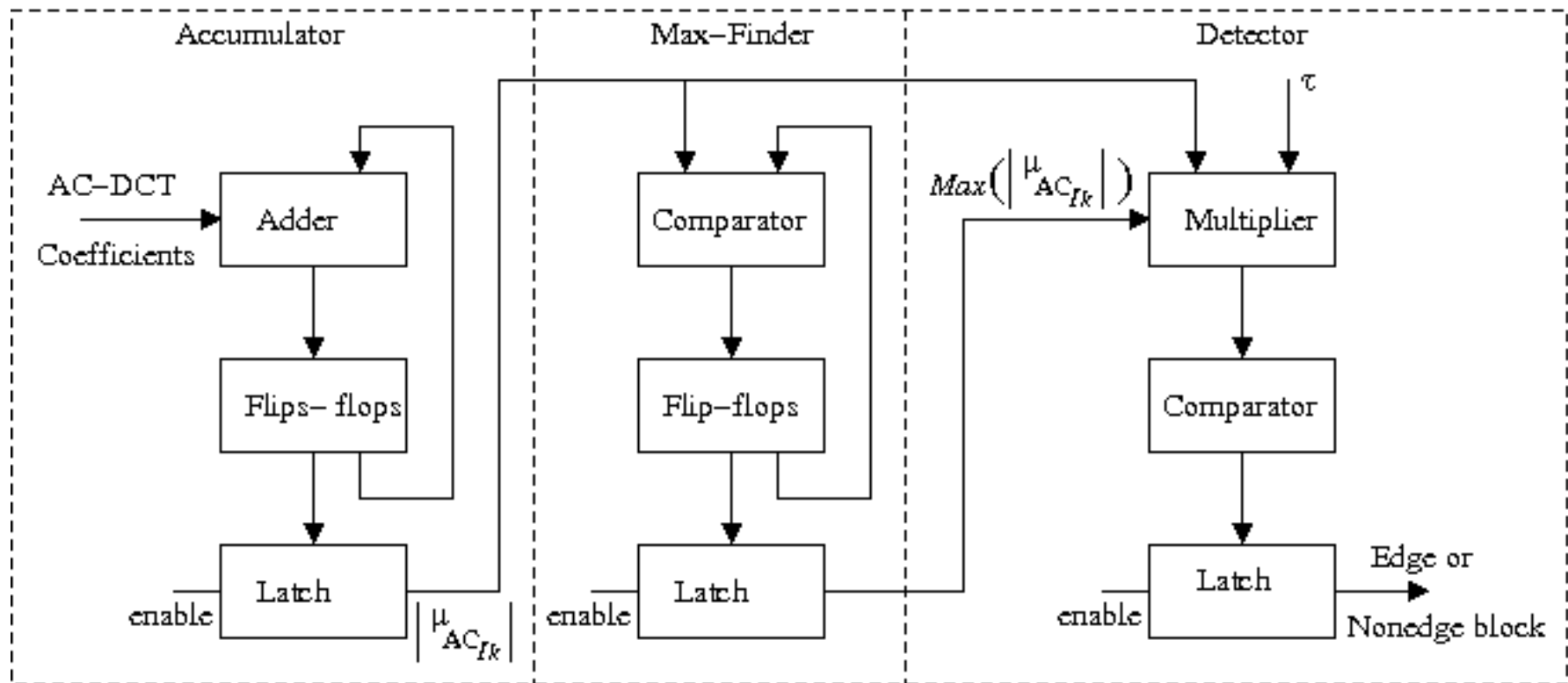


The Proposed Architecture (Edge Detection Module)

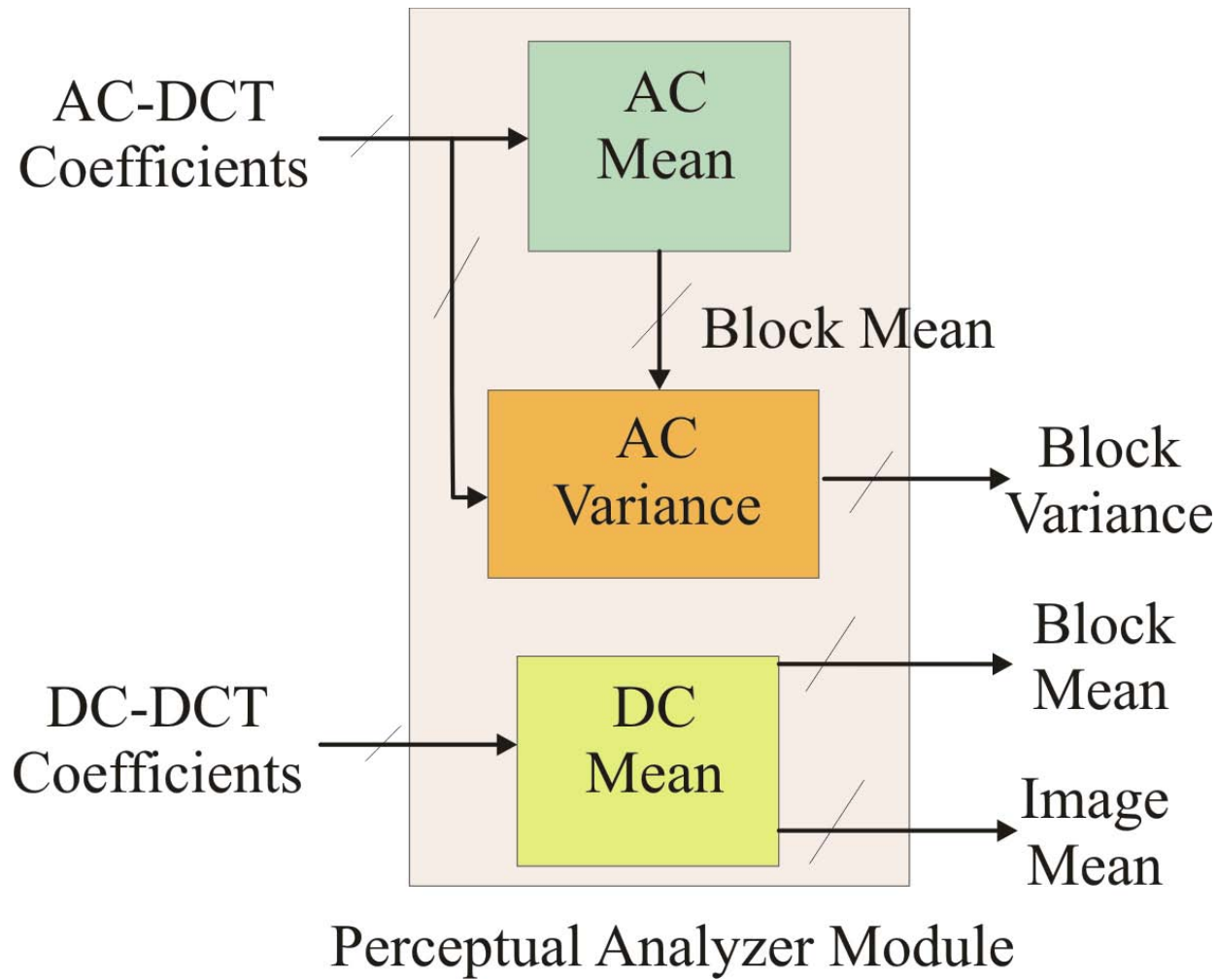


- Compute from AC-DCT:
$$\mu_{AC_{I_k}} = \frac{1}{N_B * N_B} \sum_m \sum_n |c_{I_k}(m, n)|$$
- Find the maximum:
$$|\mu_{AC_{Im_{ax}}}| = \text{Max} (|\mu_{AC_{I_k}}|)$$
- Declare edge block if:
$$|\mu_{AC_{I_k}}| > \tau |\mu_{AC_{Im_{ax}}}|$$

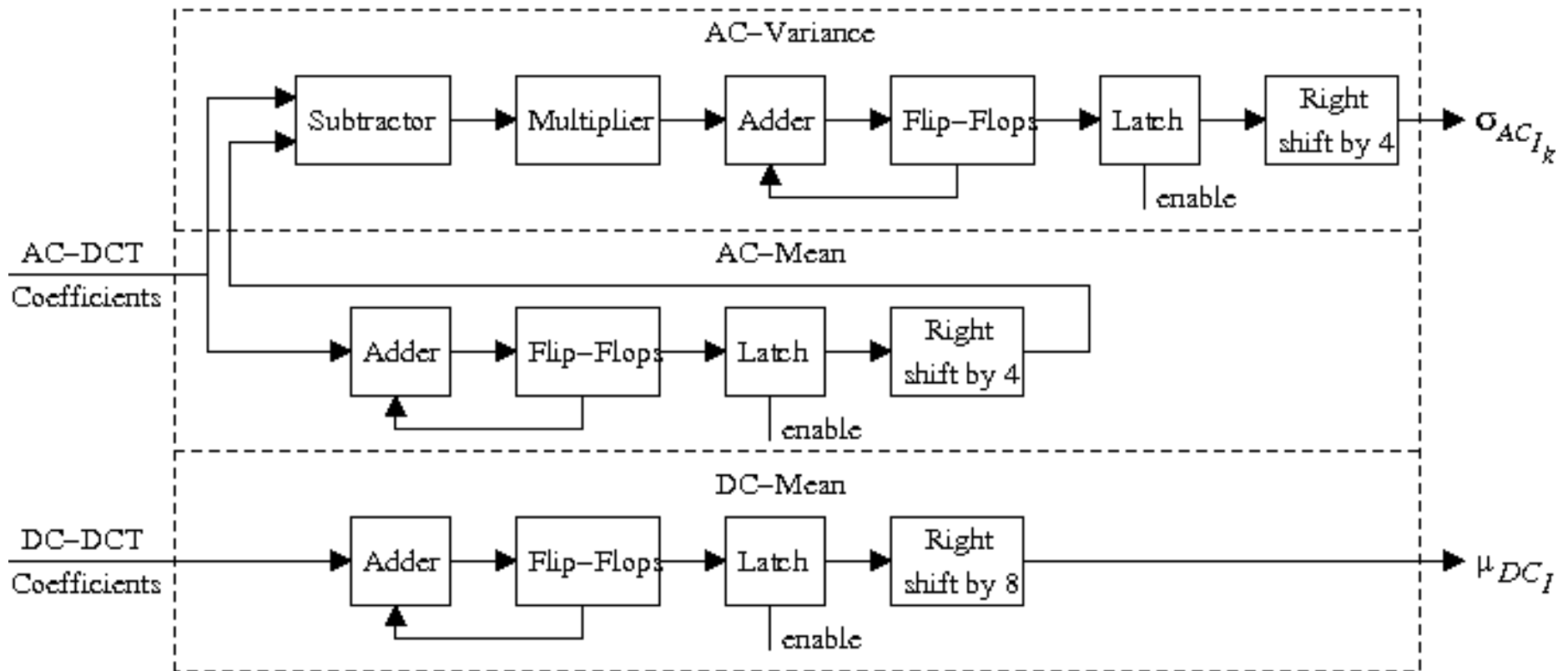
The Proposed Architecture (Edge Detection Module)



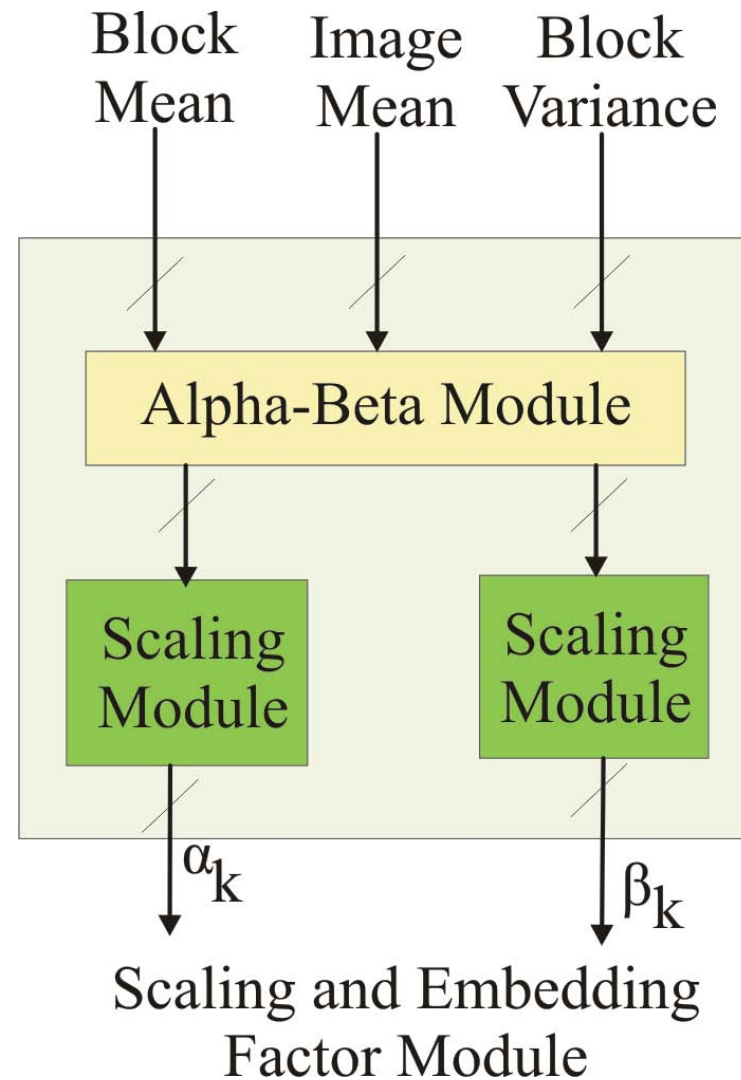
The Proposed Architecture (Perceptual Analyzer Module)



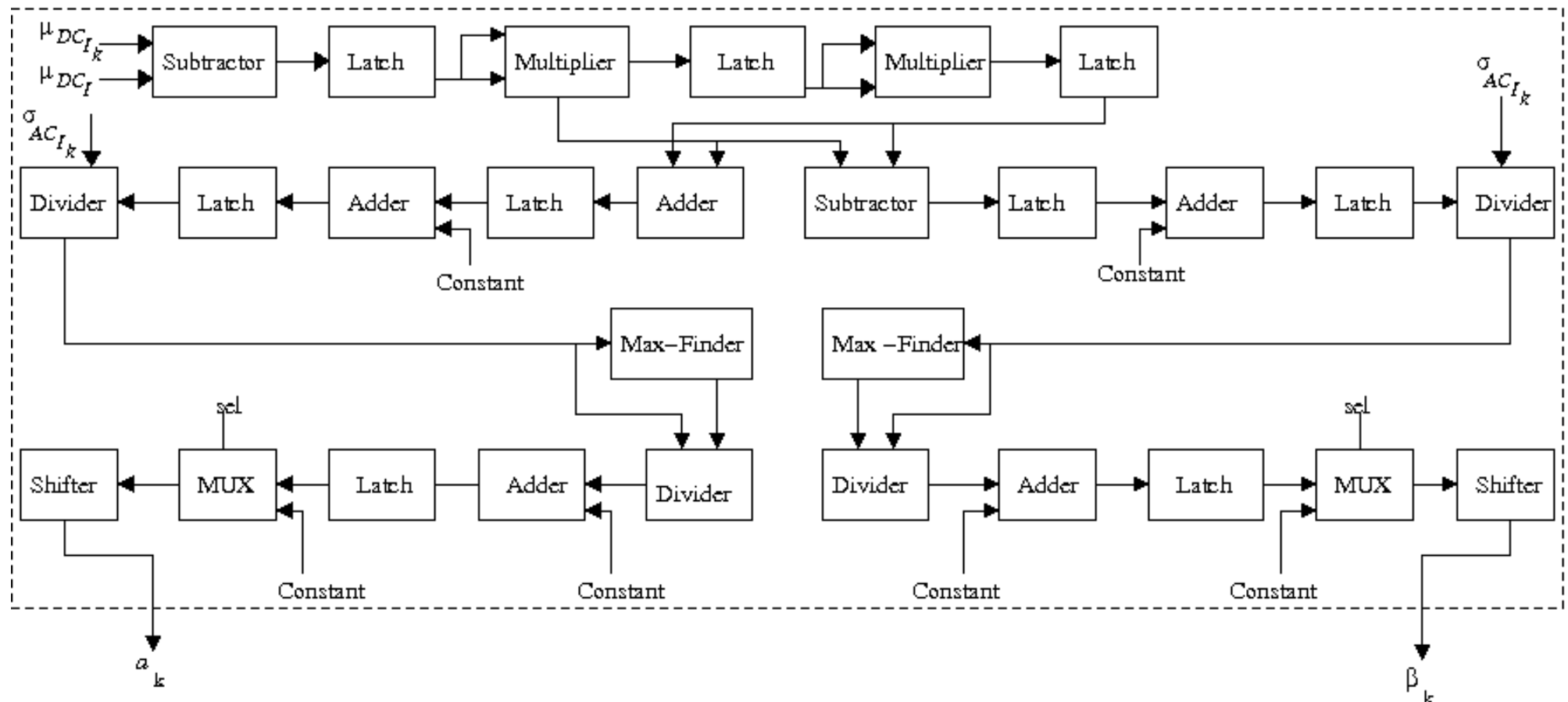
The Proposed Architecture (Perceptual Analyzer Module)



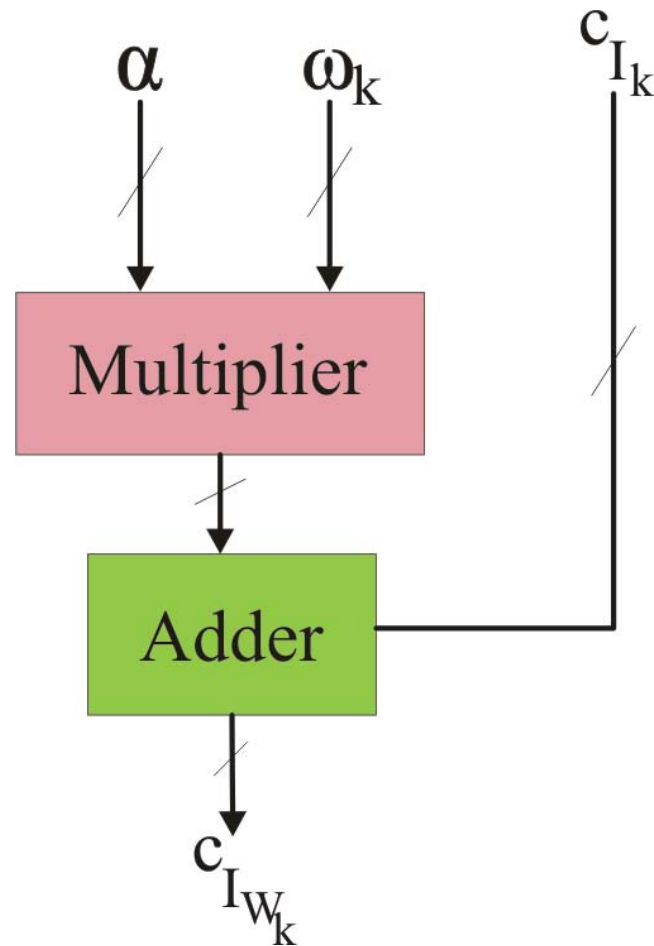
The Proposed Architecture (Scaling and Embedding Factor Module)



The Proposed Architecture (Scaling and Embedding Factor Module)



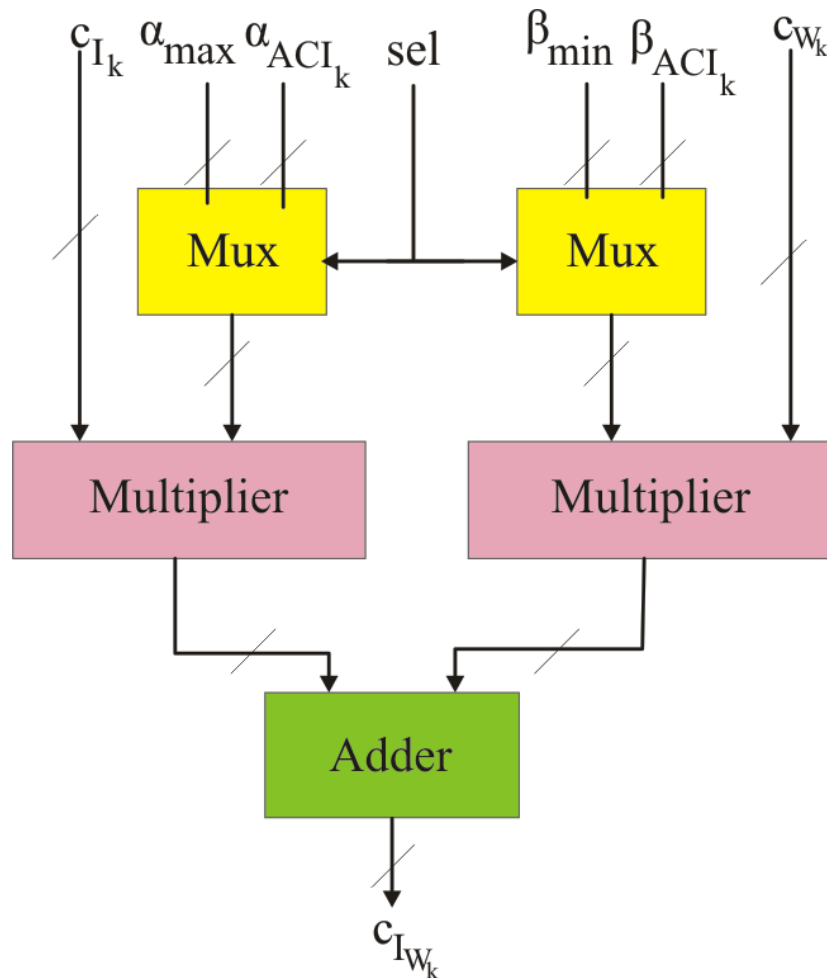
The Proposed Architecture (Invisible Insertion Module)



Invisible insertion process:

$$c_{I_{W_k}} = c_{I_k} + \alpha \omega_k$$

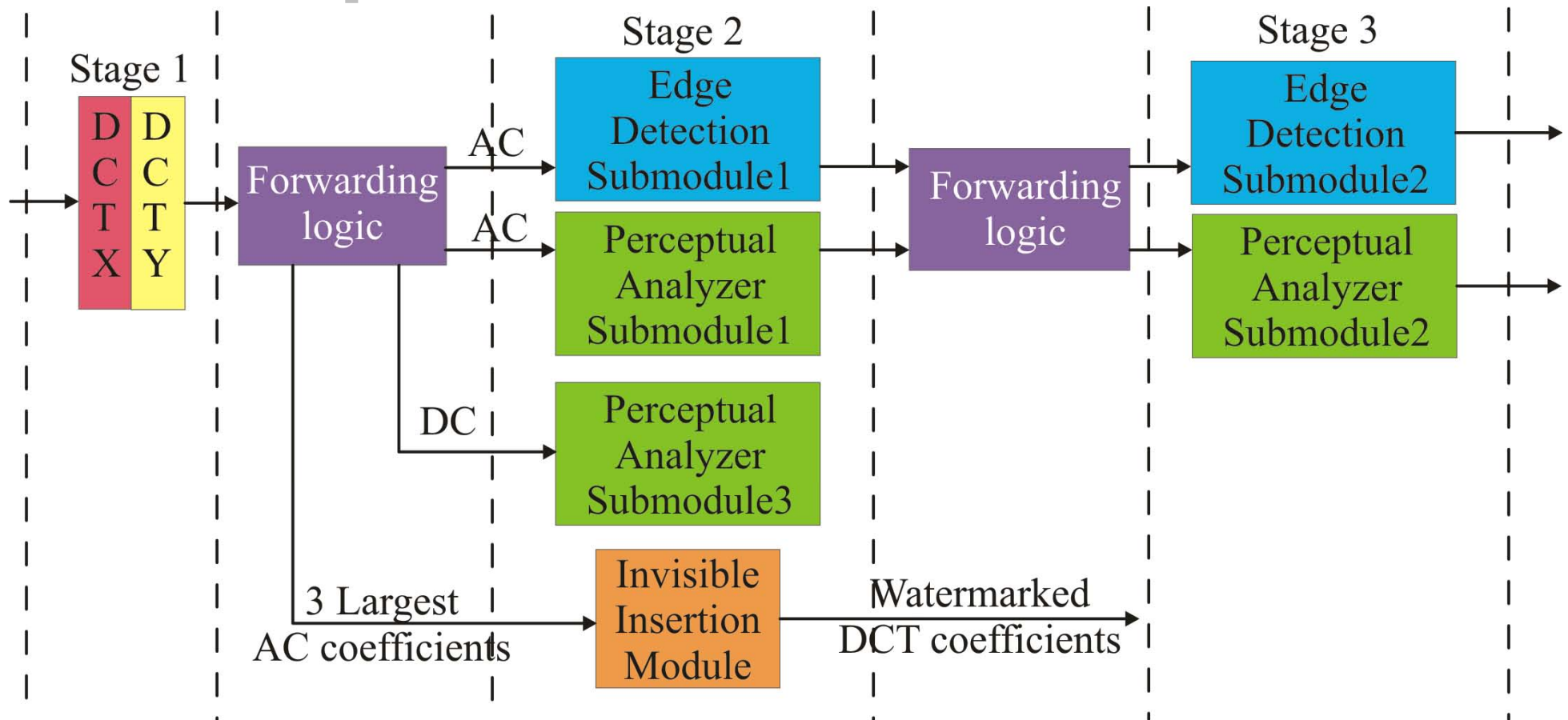
The Proposed Architecture (Visible Insertion Module)



Visible insertion process:

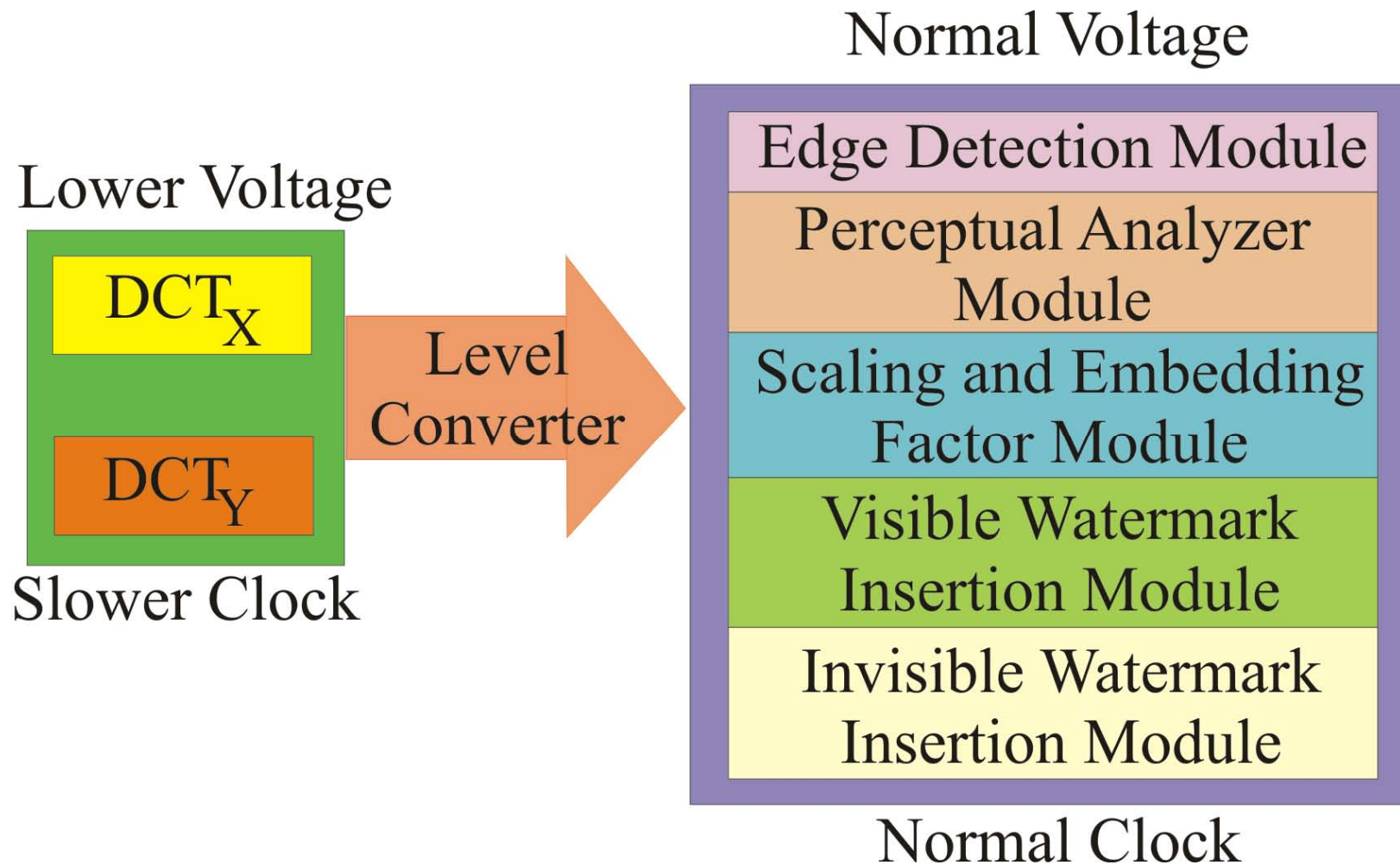
$$c_{I_{W_k}} = \alpha_k c_{I_k} + \beta_k c_{W_k}$$

The Proposed Architecture: Pipeline and Parallelism



- The visible architecture has 3 stage pipeline and the invisible architecture has 2 stage pipeline.

The Proposed Architecture: Dual Voltage and Frequency

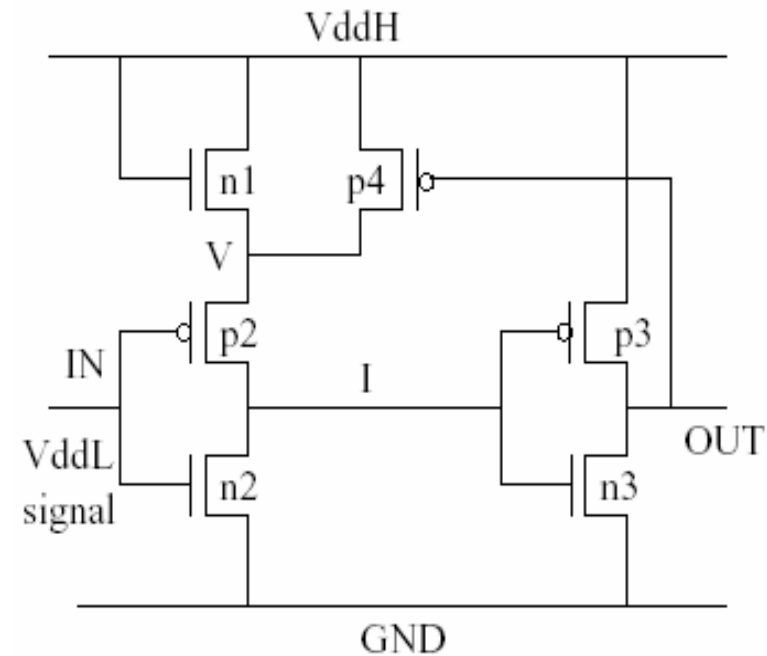
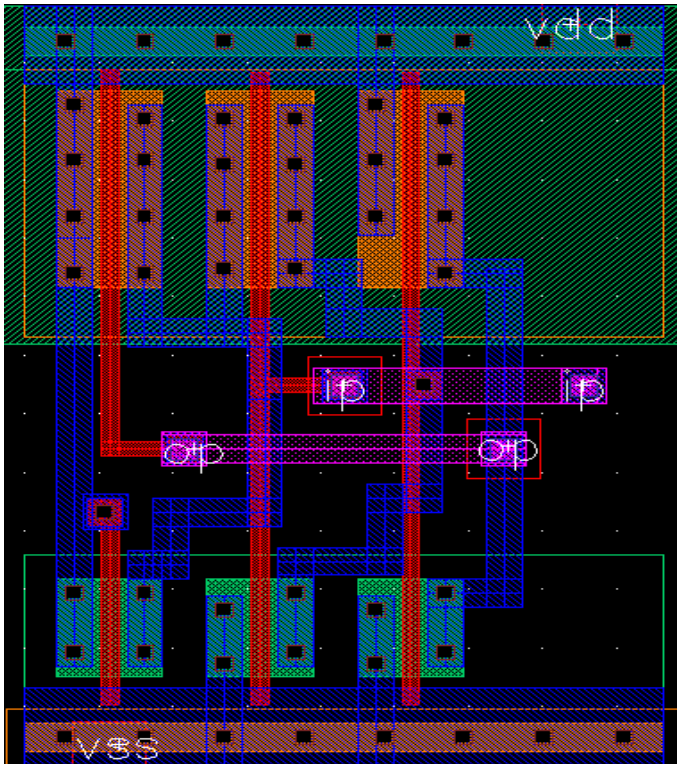


Dual Voltage: Level Converters

- Level converters required to step up the low voltage to high voltage.
- Single supply level converter is used as it is faster, consumes less power, and needs single voltage supply only.

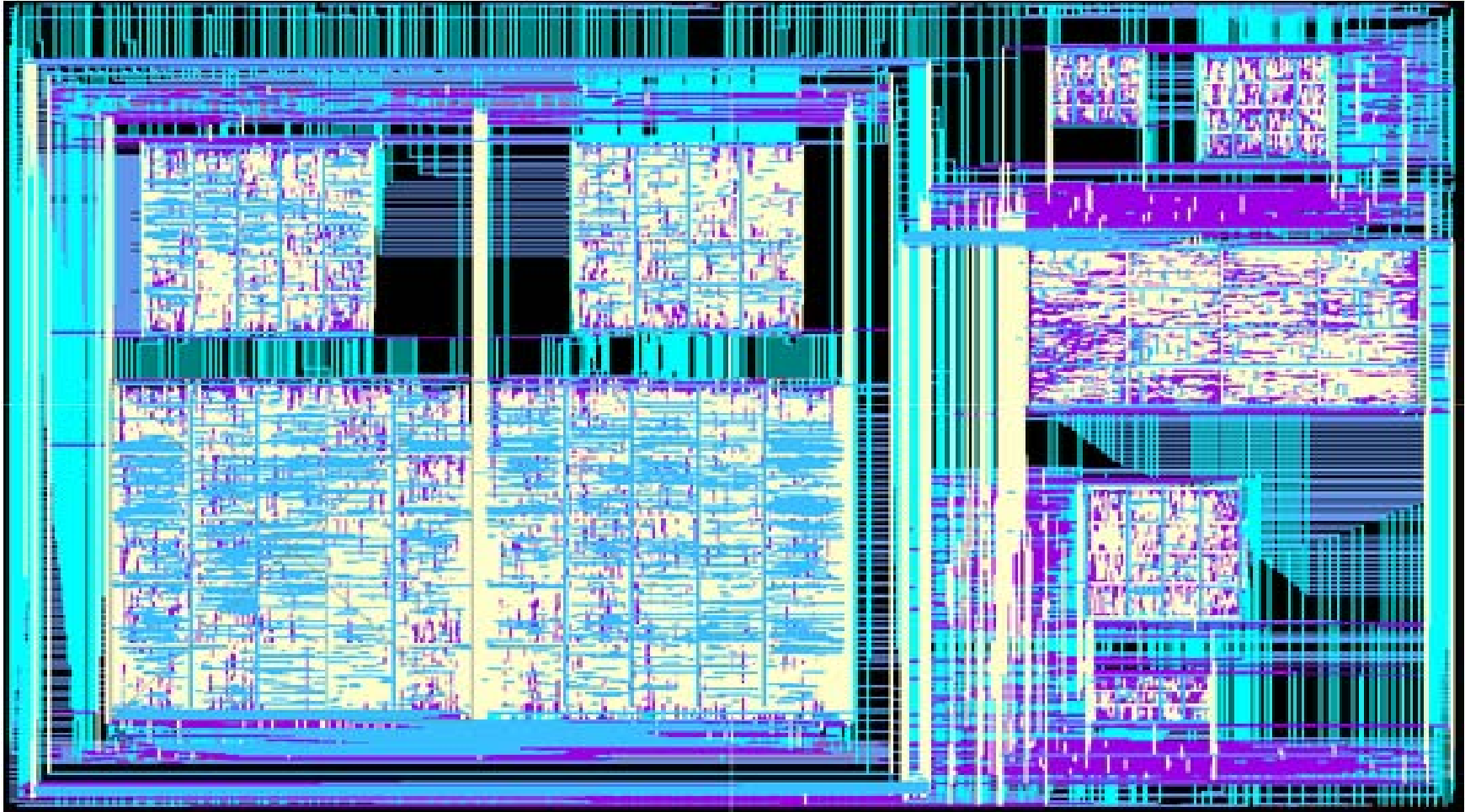
Reference: R. Puri et. al., “Pushing ASIC performance in a power envelope” in the Proceedings of the Design Automation Conference, 2003, pp. 788-793.

Single Supply Level Converter: Key Element in our Circuit



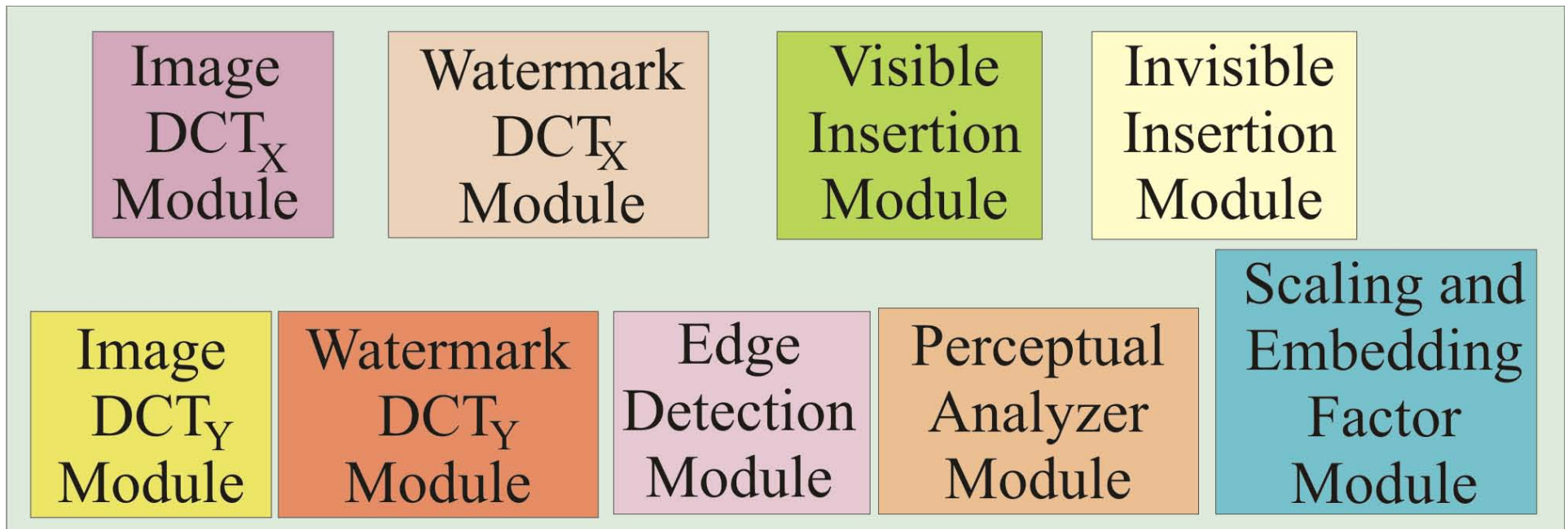
NOTE: Design of a 90nm CMOS based universal voltage level converter is currently in under progress using Cadence process design kit called gpdk_90nm.

Prototype Chip: Layout

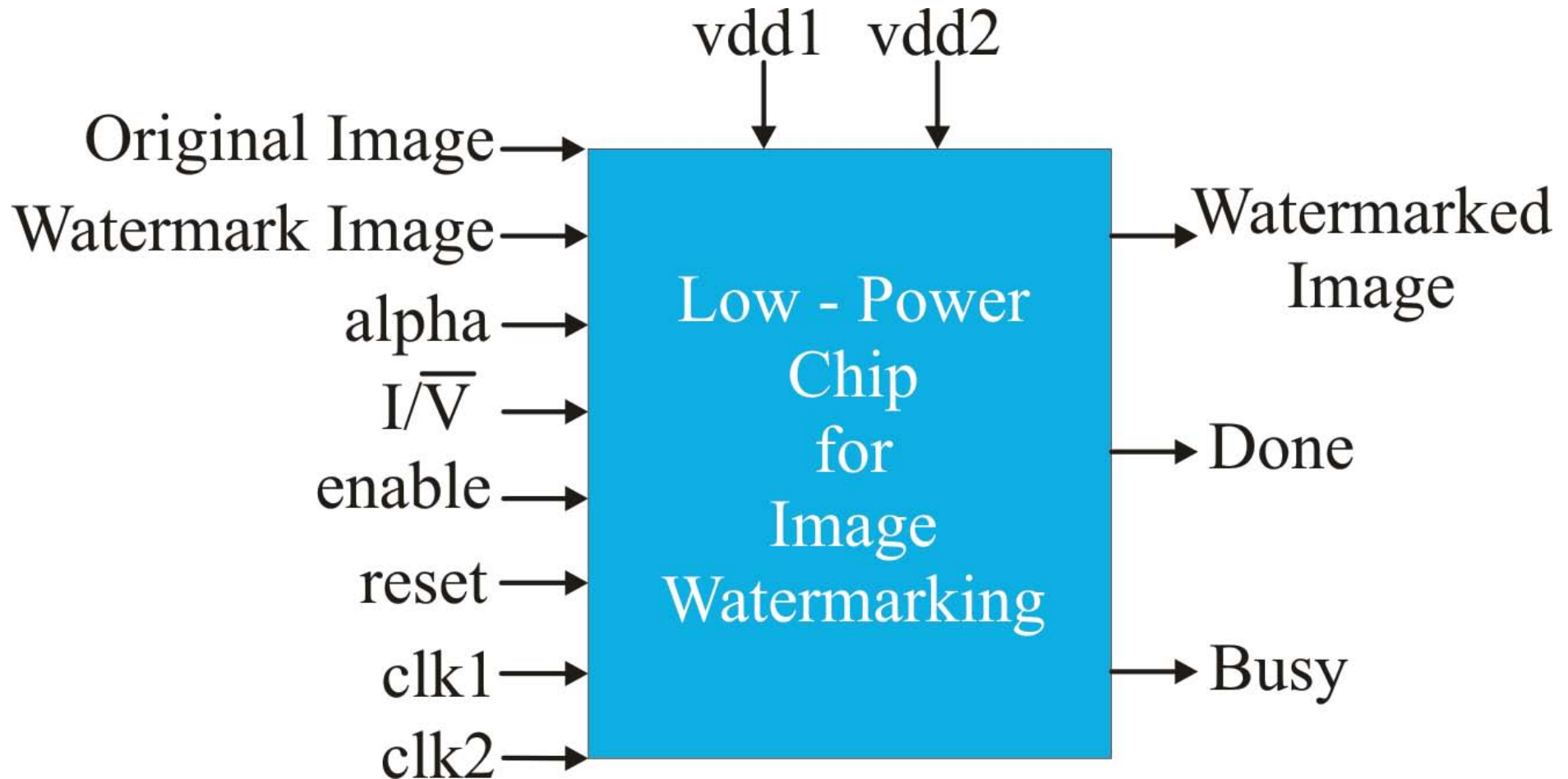


NOTE: Standard cell design style adopted. Standard cells are obtained from Virginia Tech: TSMC 0.25 μ m.

Prototype Chip: Floor Plan



Prototype Chip: Pin Diagram



Prototype Chip: Statistics

Technology: TSMC 0.25 μ m

Total Area : 16.2 sq mm

Dual Clocks: 284MHz and 71MHz

Dual Voltages: 2.5V and 1.5V

No. of Transistors: 1.4million

Power Consumption: 0.3mW

NOTE: Lowest power consuming watermarking chip available at present.

Related Works

(Hardware Systems/Circuits)

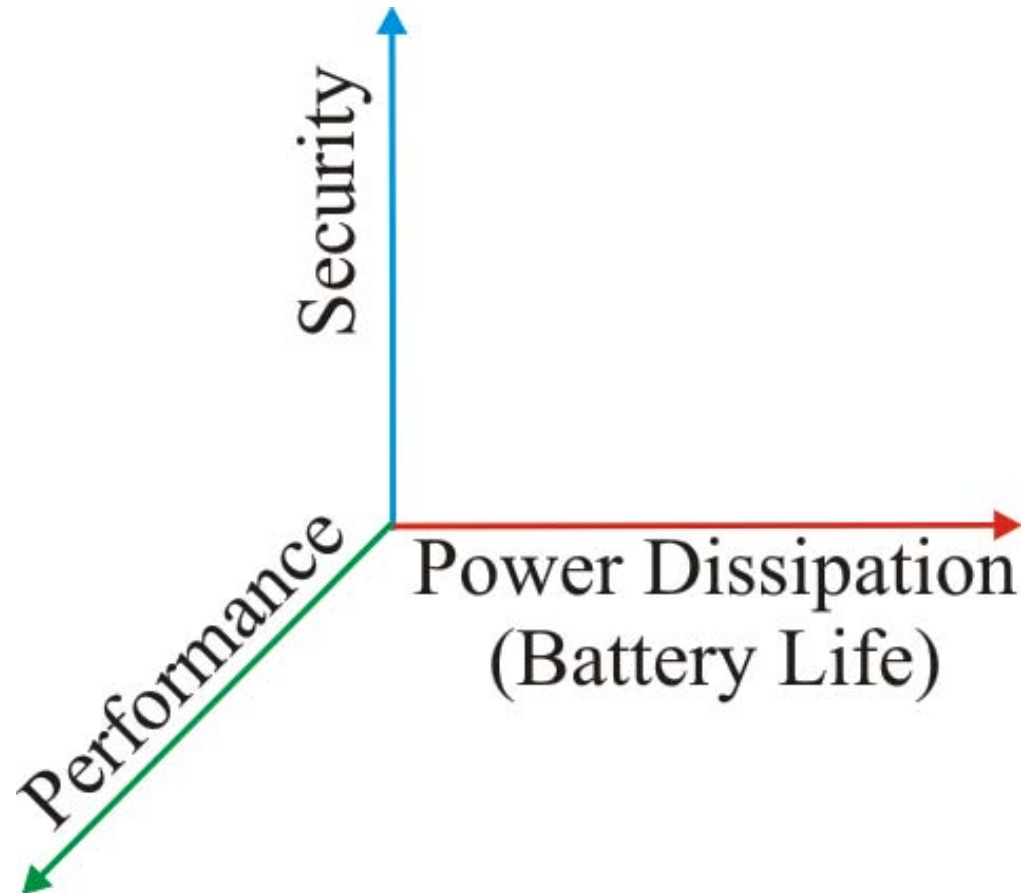
Work	Type	Target Object	Domain	Technology	Chip Power
Strycker, 2000	Invisible Robust	Video	Spatial	NA	NA
Tsai and Lu 2001	Invisible Robust	Video	DCT	0.35 μ m	62.8 mW
Mathai, 2003	Invisible Robust	Image	Wavelet	0.18 μ m	NA
Mohanty 2003	Robust Fragile	Image	Spatial	0.35 μ m	2.05 mW

Research Challenges for Security, Power, and Performance Tradeoffs

Secure SoC Design: Two Modes

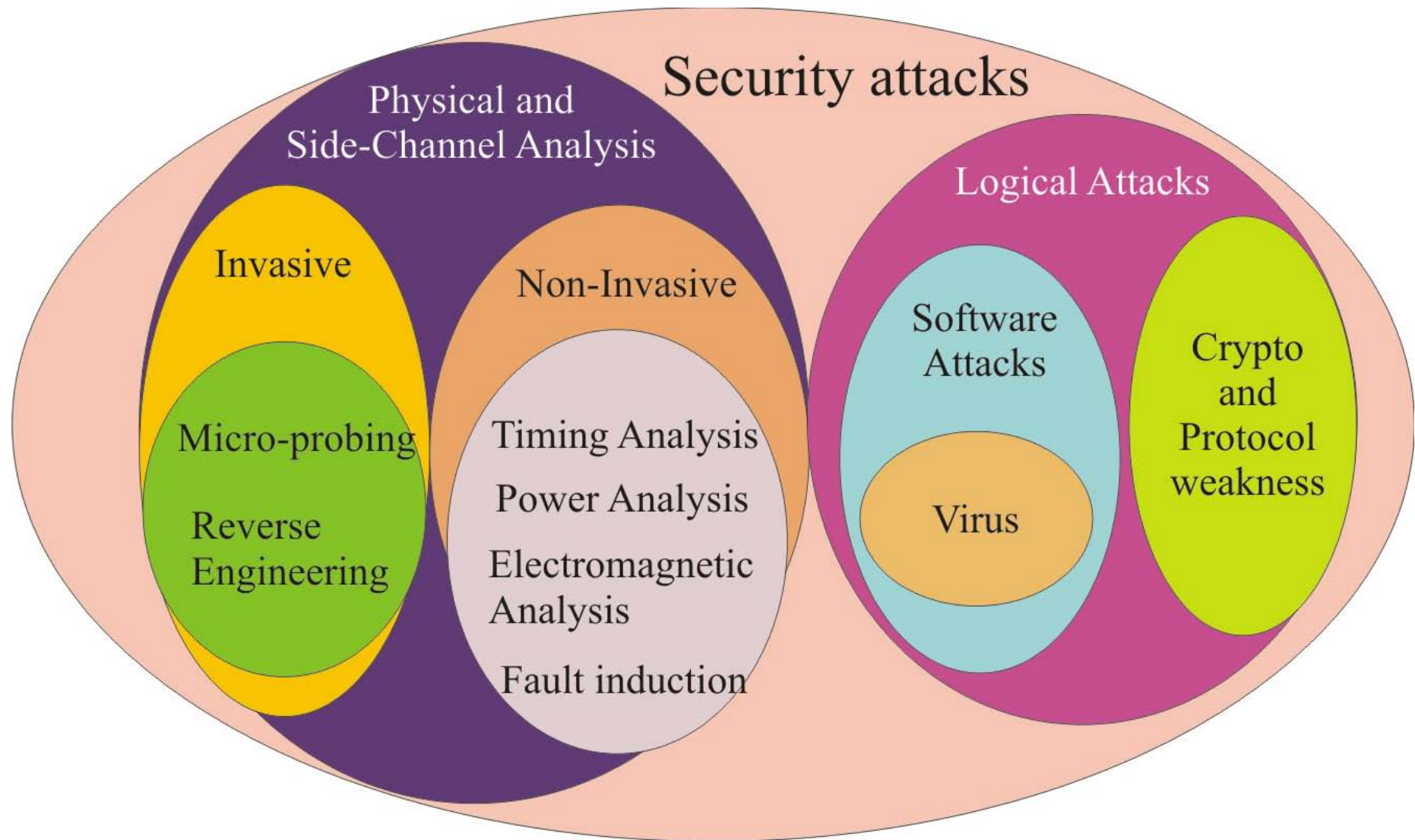
- Addition of DRM features in SoC:
 - ❑ Algorithms
 - ❑ Protocols
 - ❑ Architectures
 - ❑ Accelerators / Engines
- Consideration of DRM as a dimension in the design flow:
 - ❑ New design methodology
 - ❑ Design automation or computer aided design (CAD) tools for fast design space exploration.

Secure SoC Design Space Exploration



- Multidimensional design space, 3 are shown.
- More the security processing more the energy consumption and slower the performance.

Different Forms of Attacks on SoCs

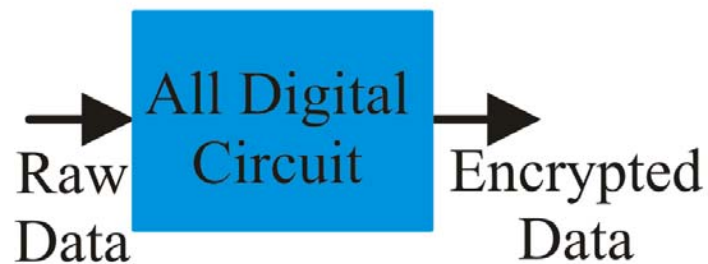


Secure Digital Camera: AMS-SoC Research Challenges

- Development of hardware amenable algorithms.
- Building efficient VLSI architectures.
- Hardware-software co-design for security, power, and performance tradeoffs.
- Analog mixed-signal system-on-a-chip (AMS-SoC) design for security, power, and performance tradeoffs.

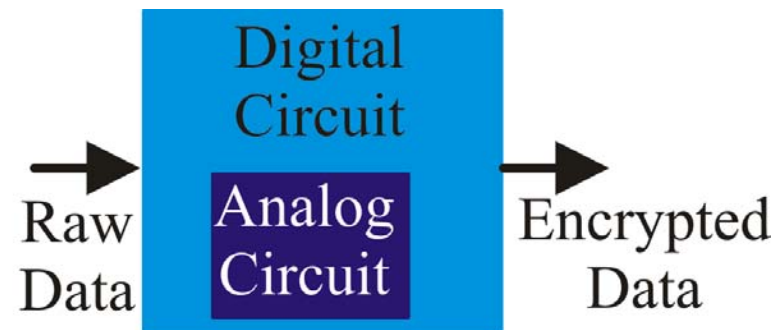
Analog-Digital Mixed-Signal Design

- A side channel attack is any attack based on information gained from the physical implementation of an encryption system.
- Static CMOS based circuit implementation are vulnerable to such attacks.



(a) Digital

Vulnerable to side channel attack.



(b) Mixed-Signal

May abstract switching activity and reduce information leaking.

Hardware-Software Co-Design

- With the same philosophy, hardware with embedded software based encryption system can be considered.



(a) Hardware only

Vulnerable to side channel attack.

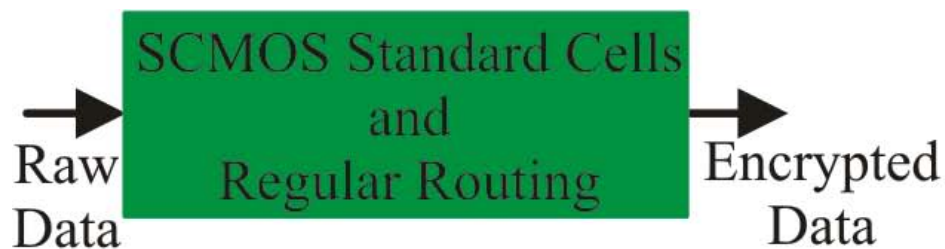


(b) Hardware-Software

May abstract switching activity and reduce information leaking.

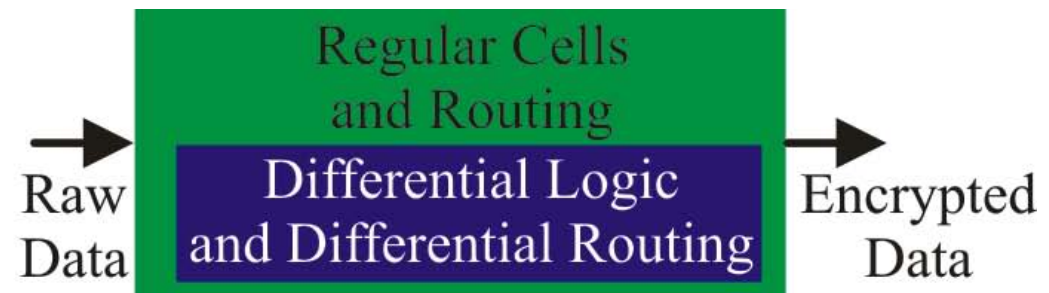
SCMOS Logic and Differential Logic Digital Circuit

- Develop logic styles and routing techniques such that power consumption per cycle is constant and capacitance charged at a node is constant.



(a) Standard SCMOS Logic

Vulnerable to side channel attack.



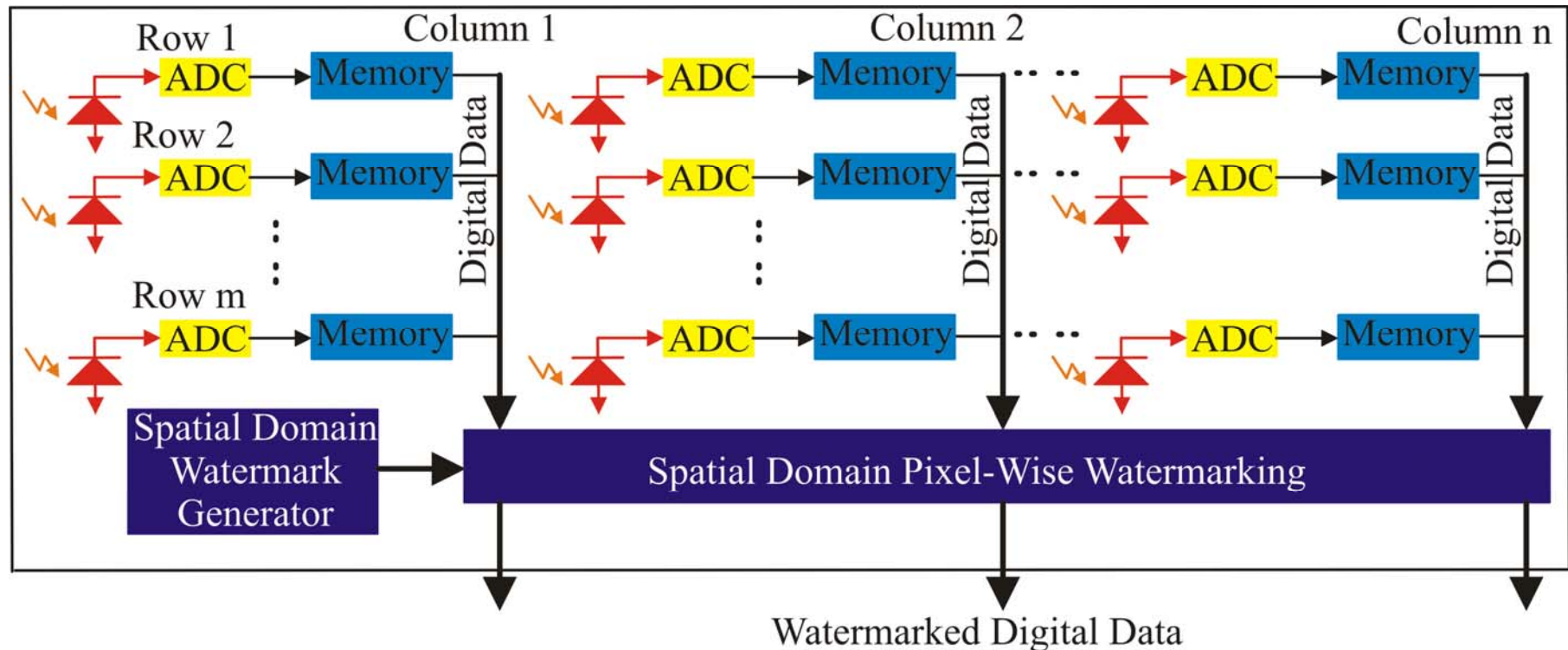
(b) Differential Logic and Routing

May abstract switching activity and reduce information leaking.

Secure Digital Camera: Alternatives

- New CMOS sensor with DRM.
- New ADC with DRM.
- Independent DRM (Watermarking, Encryption, etc.) processors.
- DRM (Watermarking, Encryption, etc) co-processor for DSP.
- New Instruction Set Architecture for RISC to support DRM at micro-architecture level.

Secure Digital Pixel Sensors

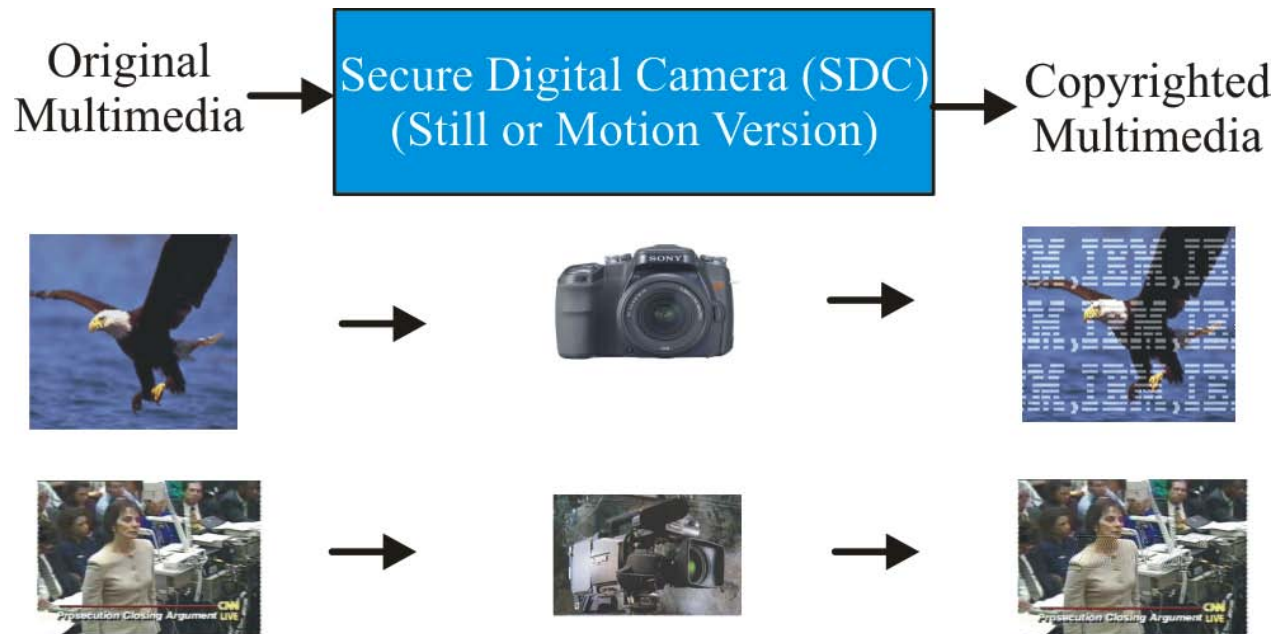


- Spatial-domain pixel-wise watermarking schemes will have less computational overhead.
- Additional circuitry will have minimal power dissipation overhead.

Secure Digital Camera (SDC): Application Scenario and Conclusions

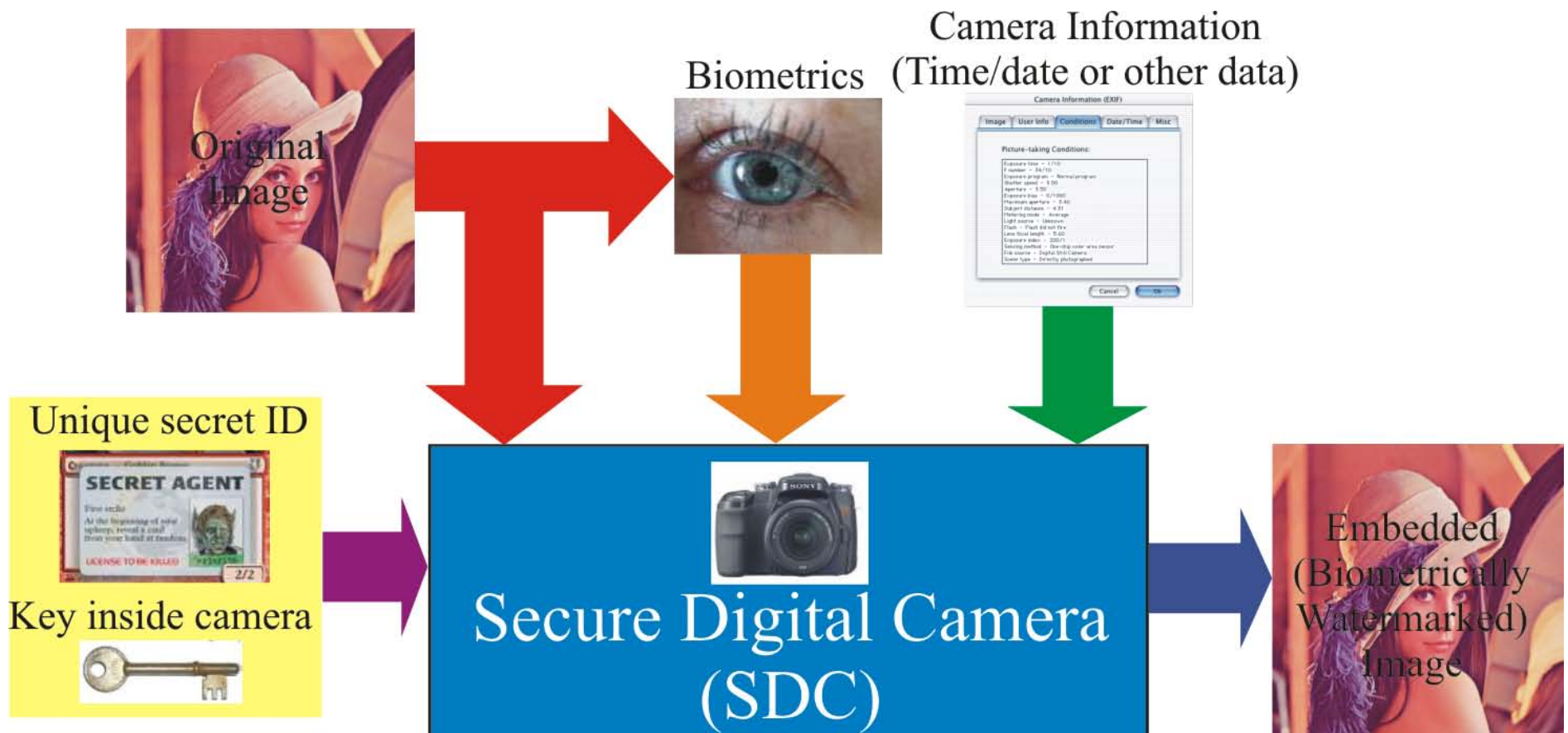
Application: Copyright Protection

- Publicly available images
- Digital Library
- DVD Video
- Digital TV Broadcasting



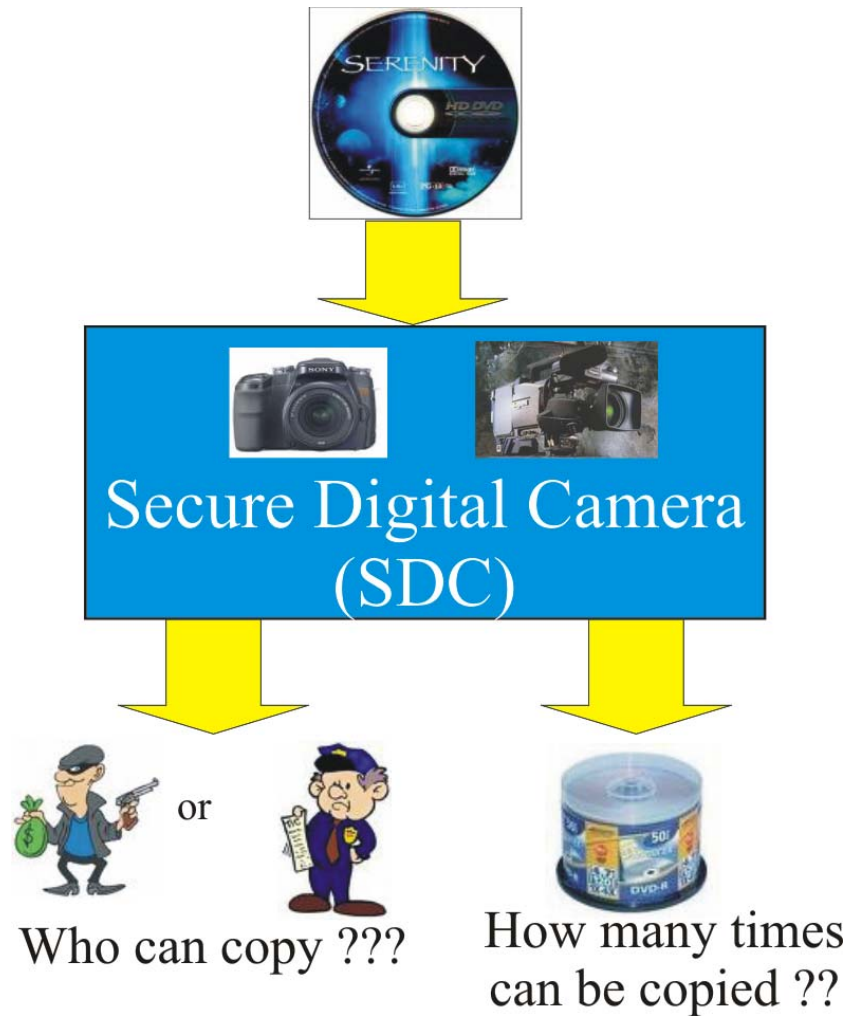
NOTE: Can enhance revenue of movie/broadcasting industry.

Application: Biometric Based Authentication



NOTE: Can be useful for homeland security, e-passport.

Application: Usage Control



NOTE: Can enhance revenue of movie industry.

Summary and Conclusions

- A low-cost low-power camera introduced that can perform DRM in real time.
- Hardware assisted DRM has several advantages over software only.
- Structure of SoCs that will realize the secure digital camera is an ongoing research.
- A low-power watermarking chip is designed that consumes 0.3mW power.
- SDC to be realized as an SoC will involve security, power, and performance tradeoffs.
- Design automation or computer-aided design (CAD) tools would be necessary for fast and automatic AMS-SoC design space exploration.

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Thank You

For more information:

<http://www.cse.unt.edu/~smohanty>