A Universal Voltage Level Converter for Multi-V_{DD} Based Low-Power Nano-CMOS Systems-on-Chips (SoCs)

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Agenda

- Introduction
- Related research works
- Design of ULC
- Simulation results at 90nm technology
- Characterization of ULC
- Custom layout design at 90nm technology
- Conclusion and future works

Introduction

- Power dissipation reduction has become a major design issue for VLSI design at nano-scale technologies.

- Sources of power dissipation
  - Dynamic power
  - Static power
  - Power dissipation due to leakage currents

- $P_{total} = s*C*V_{DD}^{2}*f + I_{sc}*V_{DD} + I_{leakage}*V_{DD}$

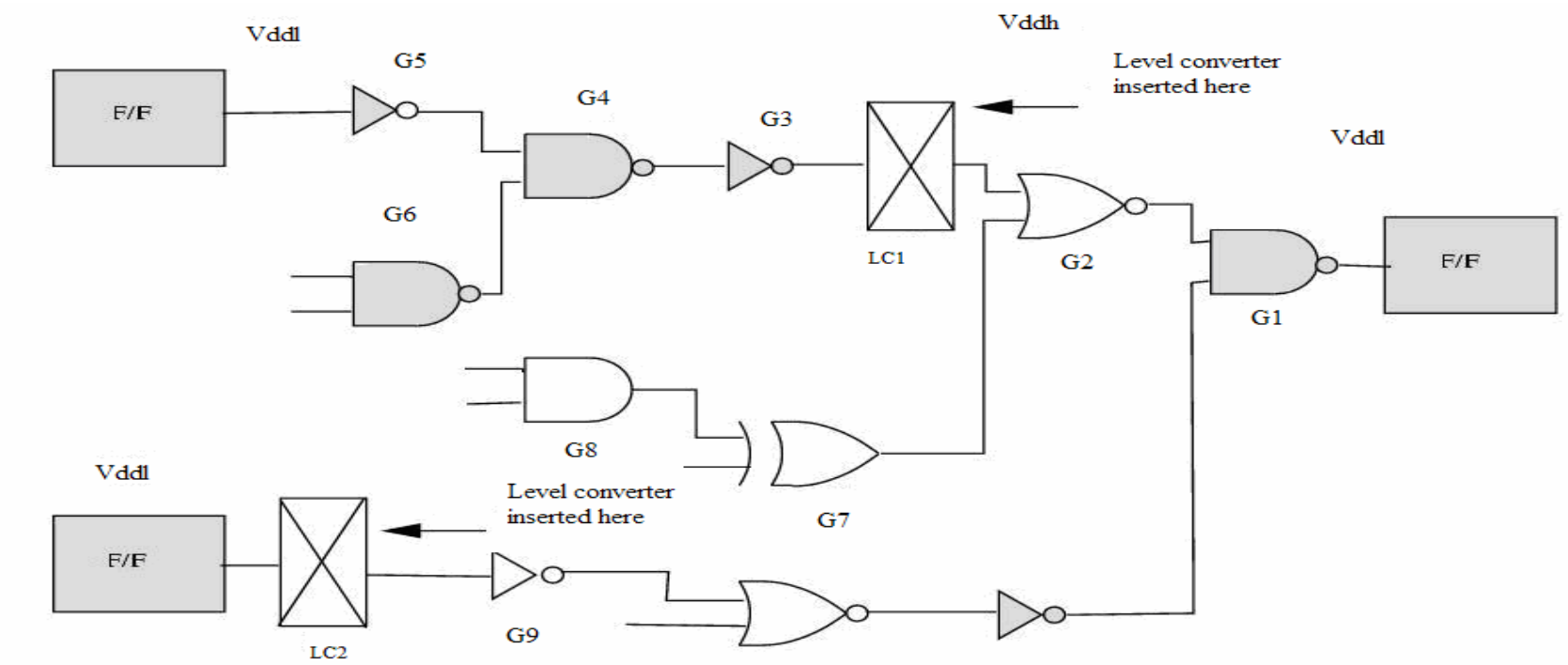
Techniques for power dissipation reduction

- Reducing the supply voltage
- Transistor sizing
- Multiple threshold voltages
- Multi-voltage supply systems

Multi-V_{DD} supply system

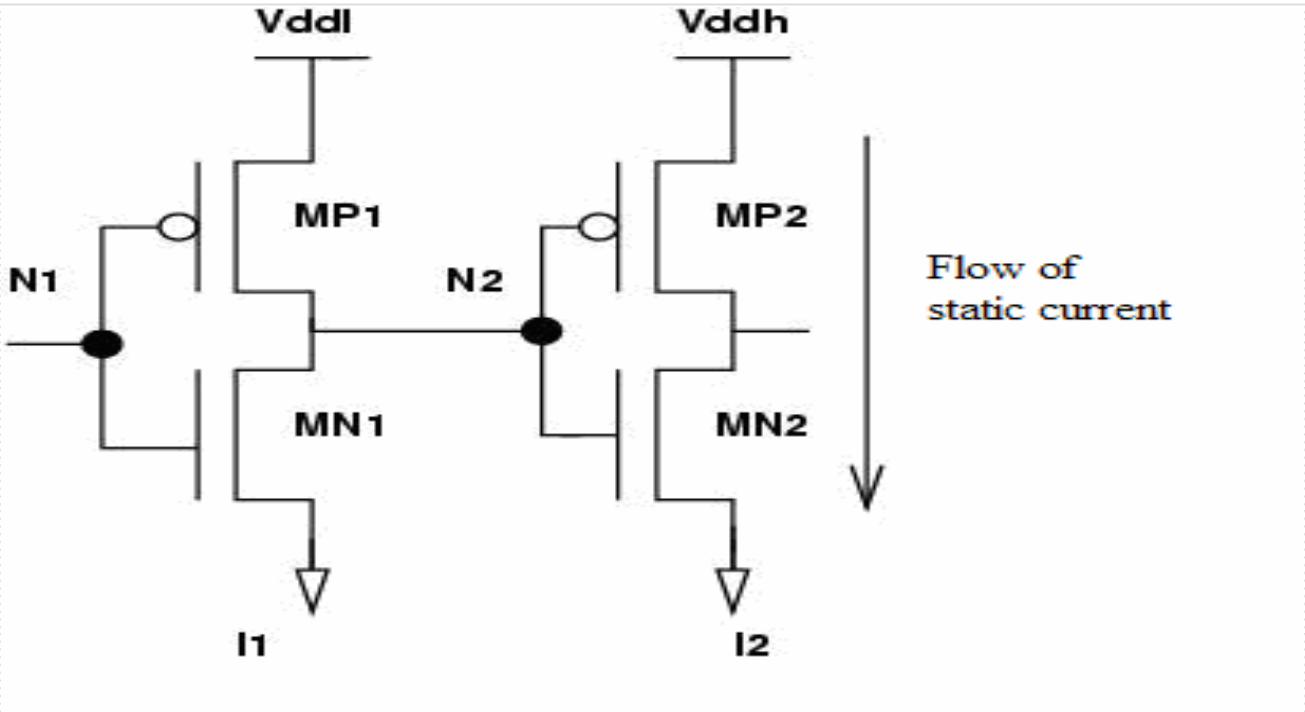
- Multiple voltage supply systems are one of the most efficient methods to reduce power dissipation
- The system is divided into voltage islands operating at different supply voltages
- Level converters are used as interface between to voltage islands
- Level converter: A circuit which changes the voltage level at its input to another level at the output side is known as a level converter

Need for level converter



Block diagram of a multi-voltage supply system demonstrating the need for level converter

Need for a level converter



Direct connection between two inverters demonstrating the need for level converter

Related research works

- Clustered voltage scaling : Allows insertion of level converters at the interface of cells at different voltages

- Extended clustered voltage scaling : Allows insertion of level converters between any gates, wherever level conversion is required

Related research work *(contd..)*

Author	Year	Technology	Type of circuit	Design approach	Power consumption	Delay
[Ishihara 2004]	2004	0.13mm	Level up converter	Level converting flip flops LCFF	----	287 ps
[Kulkarni 1999]	1999	0.13mm	Level up converter	DCVS and Keeper transistor	----	----
[Yu 2001]	2001	0.35mm	Level up Converter	Symmetrical Dual Cascode Voltage Switch	220.57 mW	----
[Sadeghi 2006]	2006	0.1mm	Level up Converter	Keeper transistor in pass transistor logic	----	----
[Kanno 2000]	2000	0.14mm	Level down converter	Differential input pair operation	----	----
[Nam-Seog 2003]	2003	0.1mm	Level up converter	Dynamic Level Converter		< 120ps

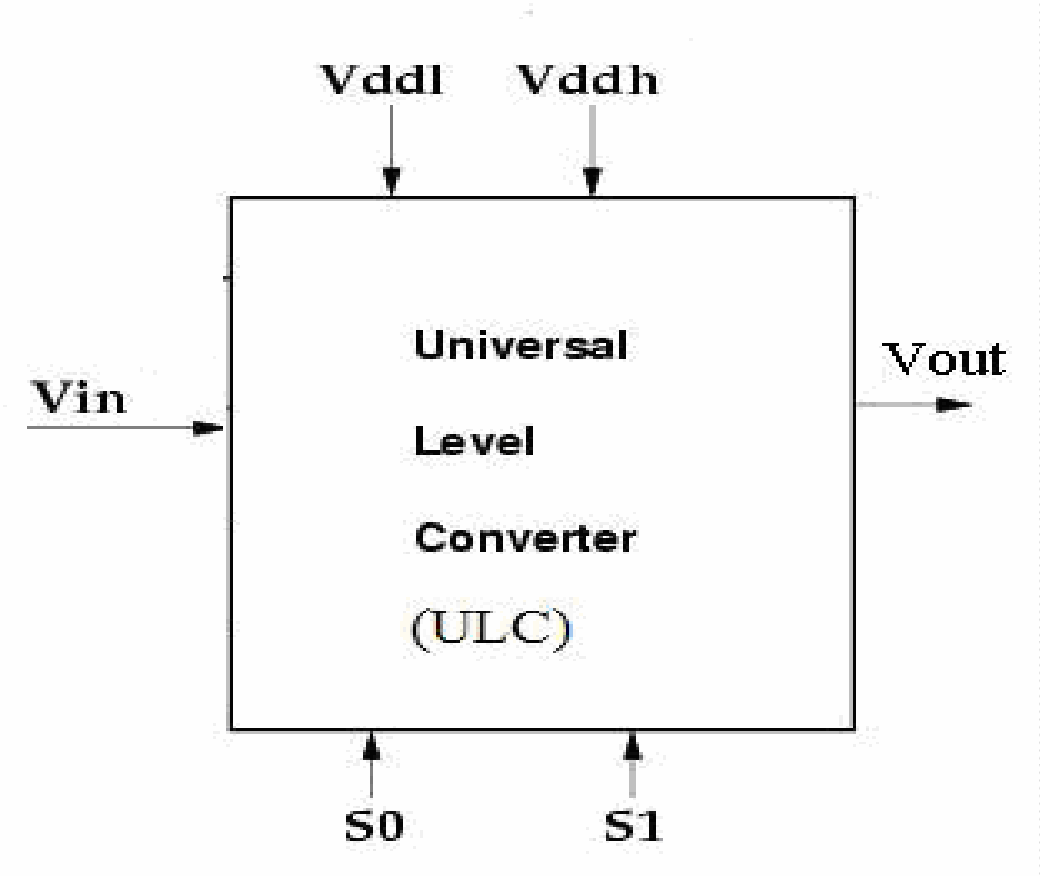
Universal Level Converter

- Level up conversion
- Level down conversion
- Blocking of signal
- Passing signal

Operations of ULC

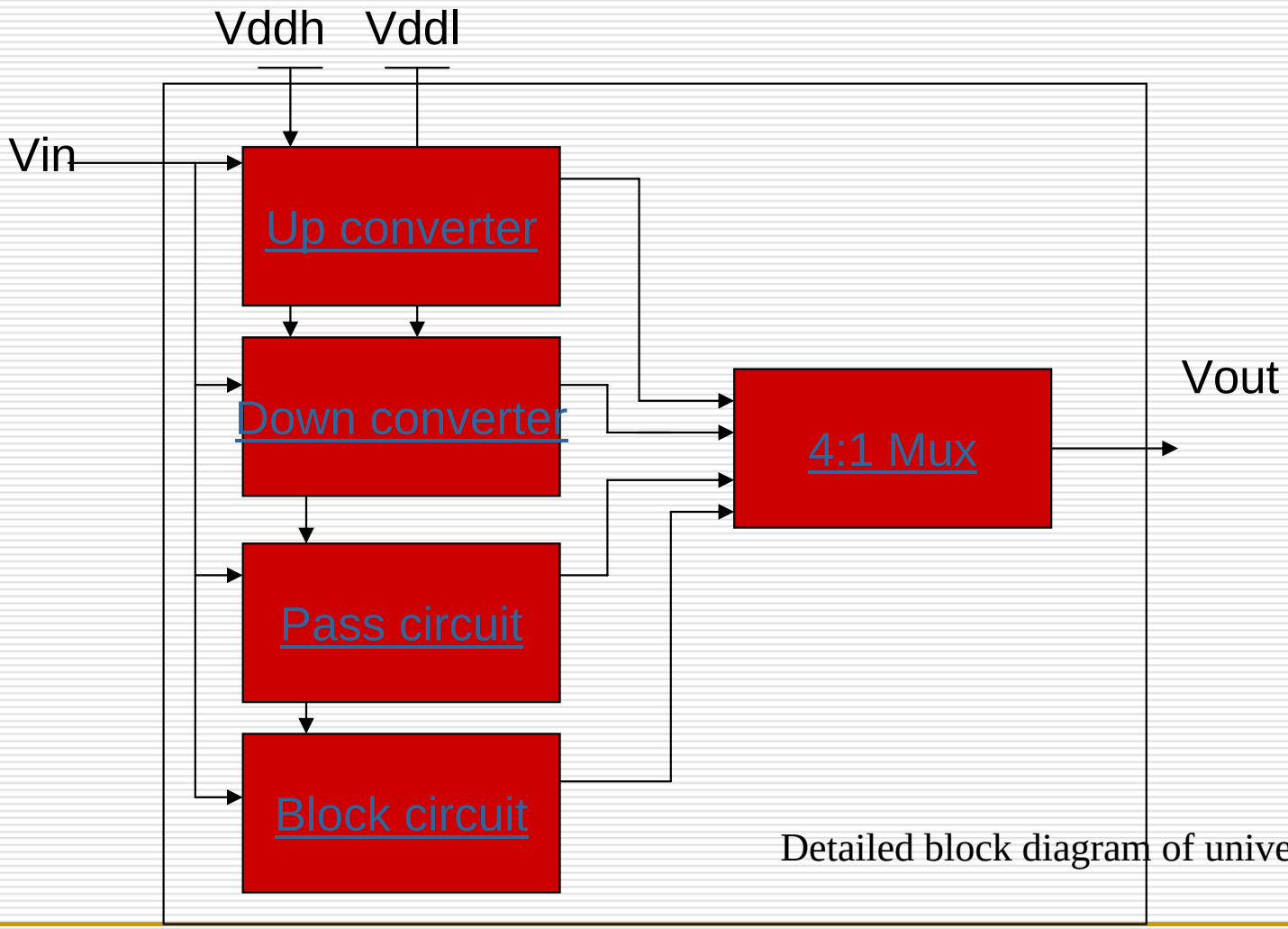
Select signal		Type of operation
s0	s1	
0	0	Passing operation
0	1	Blocking operation
1	0	Down conversion
1	1	Up conversion

Design of Universal level converter



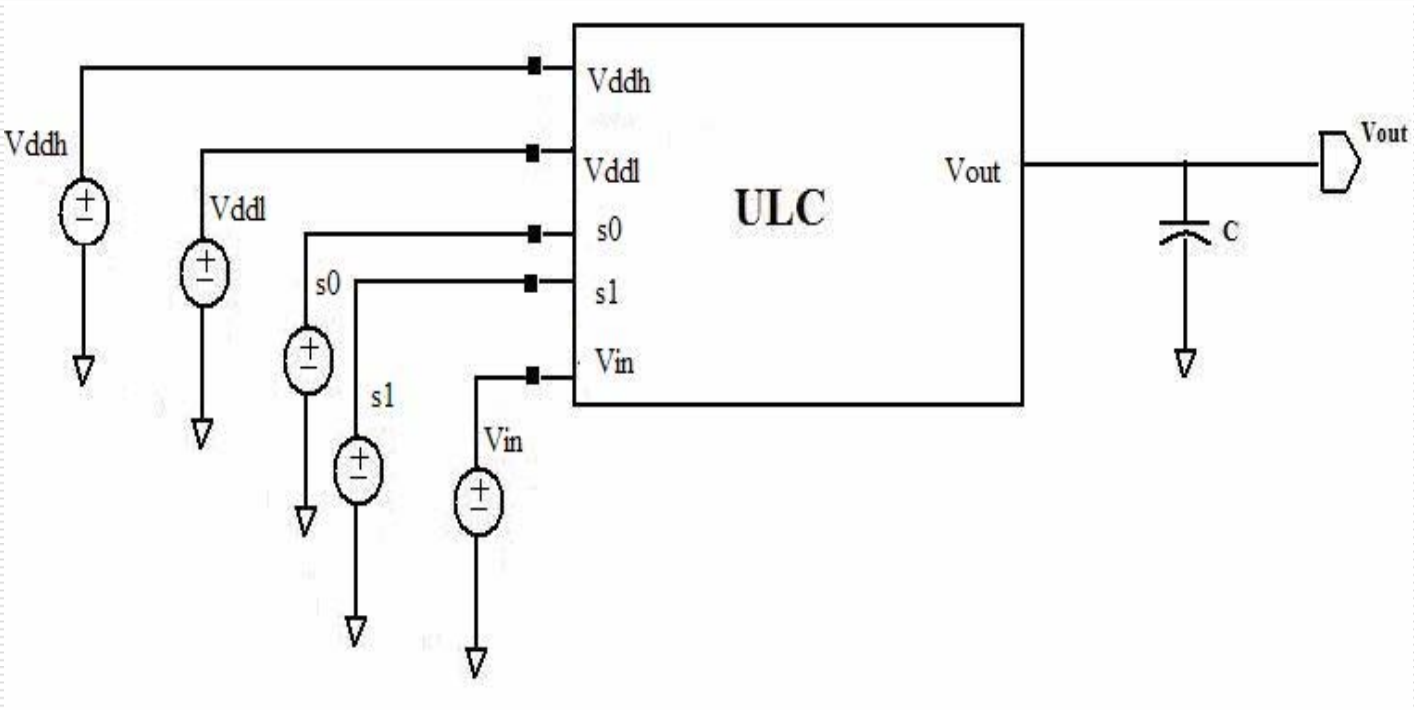
High Level view of Universal level converter proposed

(Contd..)



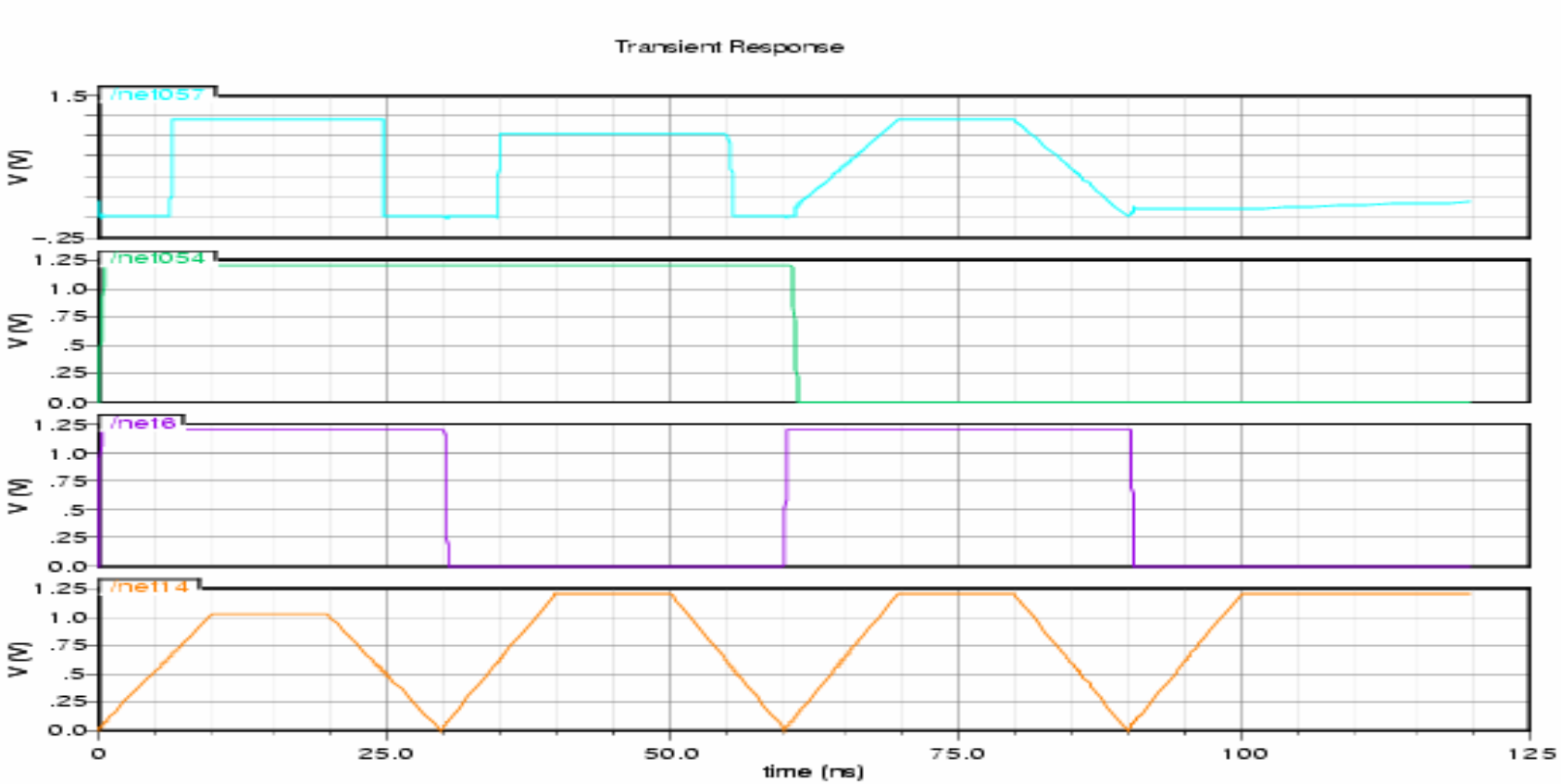
Detailed block diagram of universal level converter

Simulation test bench



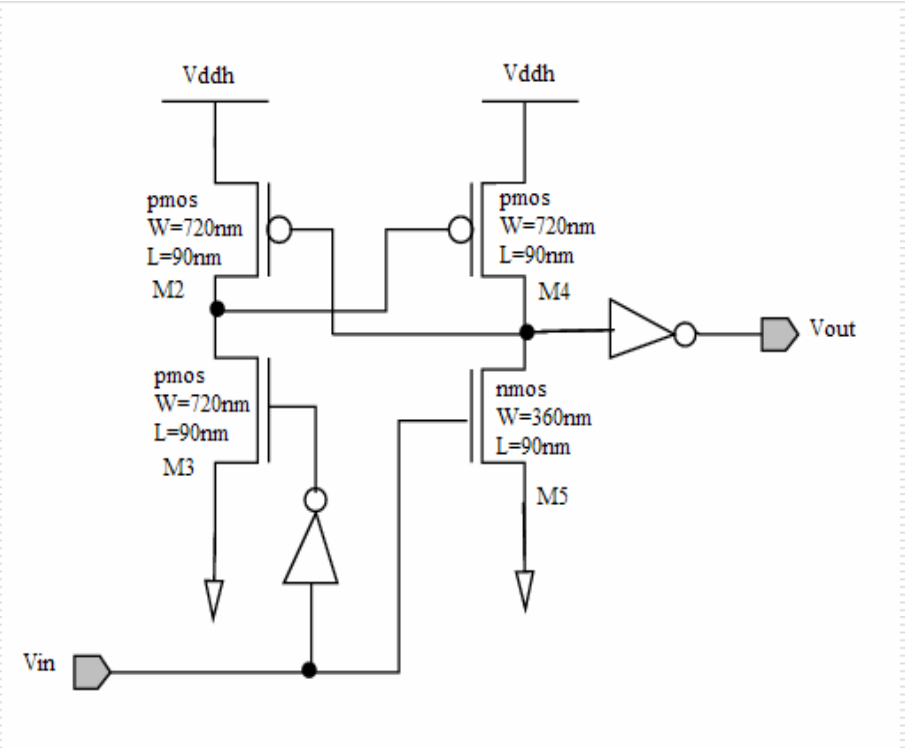
Simulation test bench of universal level converter

Simulation results of ULC

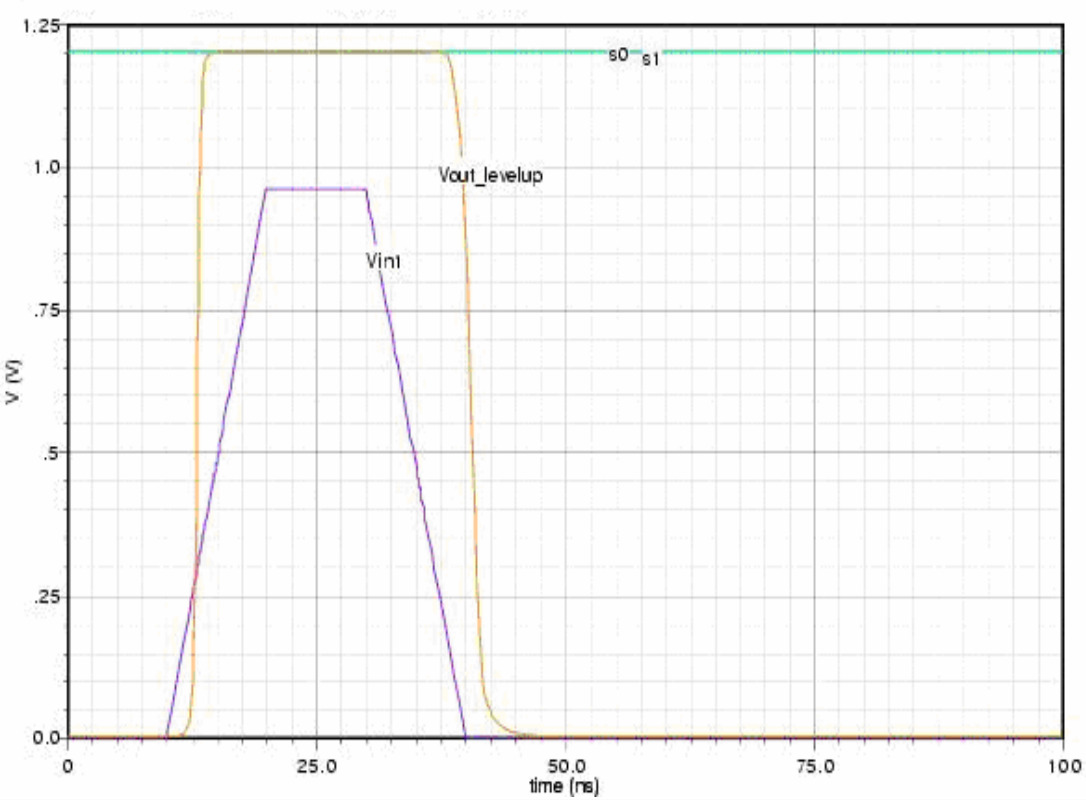


Simulation results for ULC showing the output waveforms in all modes of operation

Level up converter

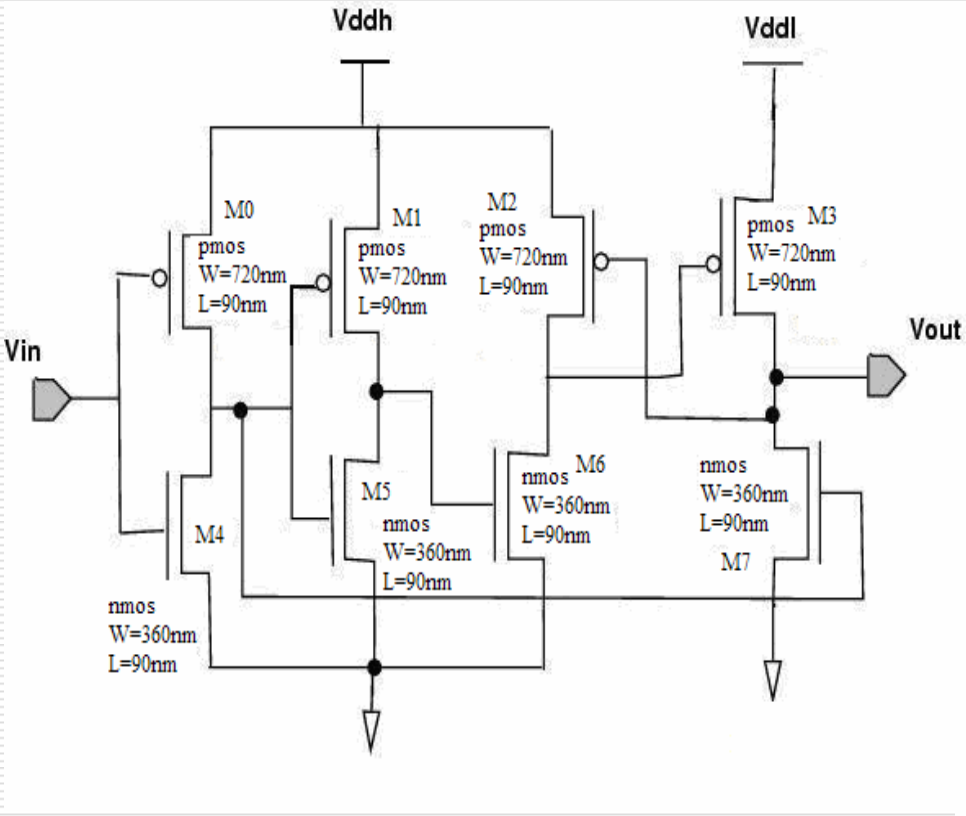


Transistor level circuit diagram of cross coupled level converter (CCLC)

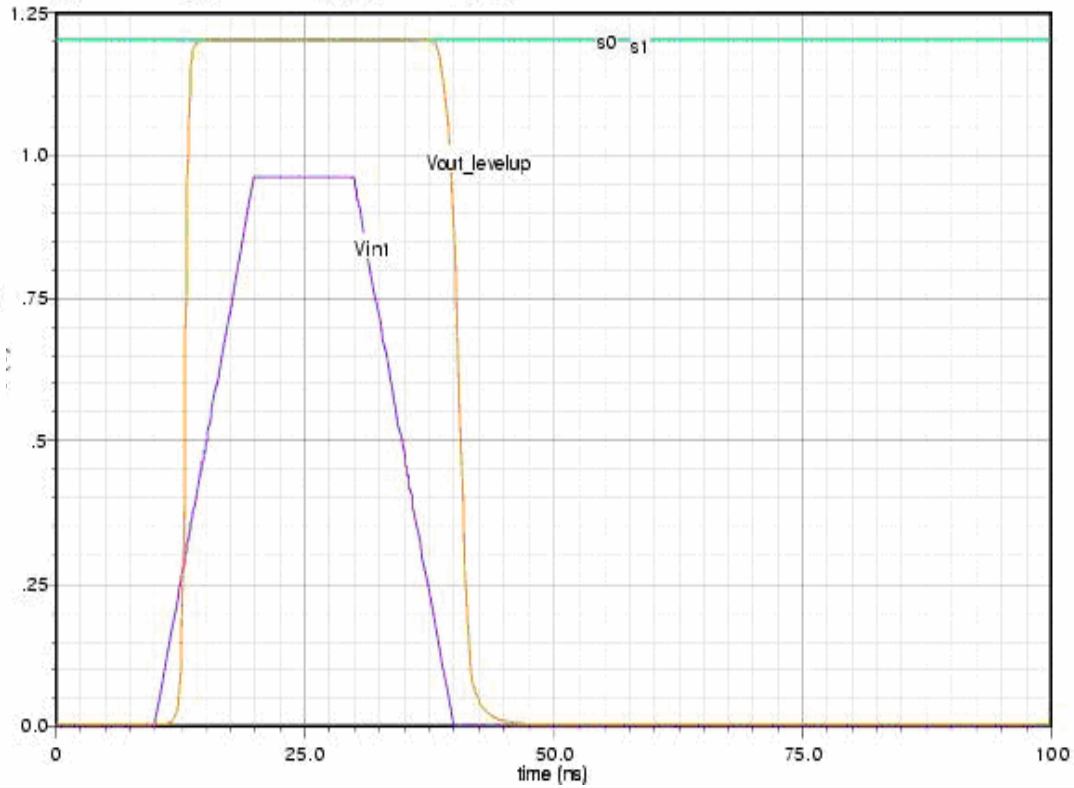


Output waveform for level up converter with Vddl = 1.02V, Vddh = 1.2V and load = 45fF.

Level down converter

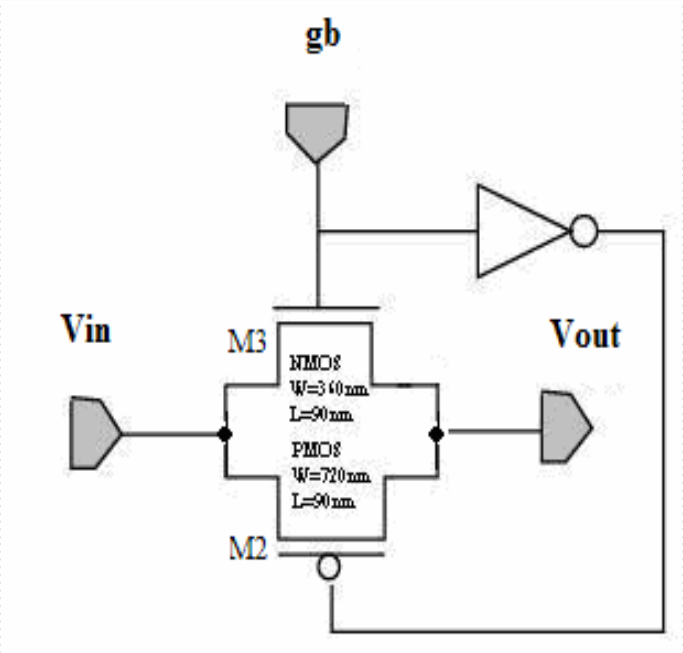


Transistor level circuit diagram of level down converter

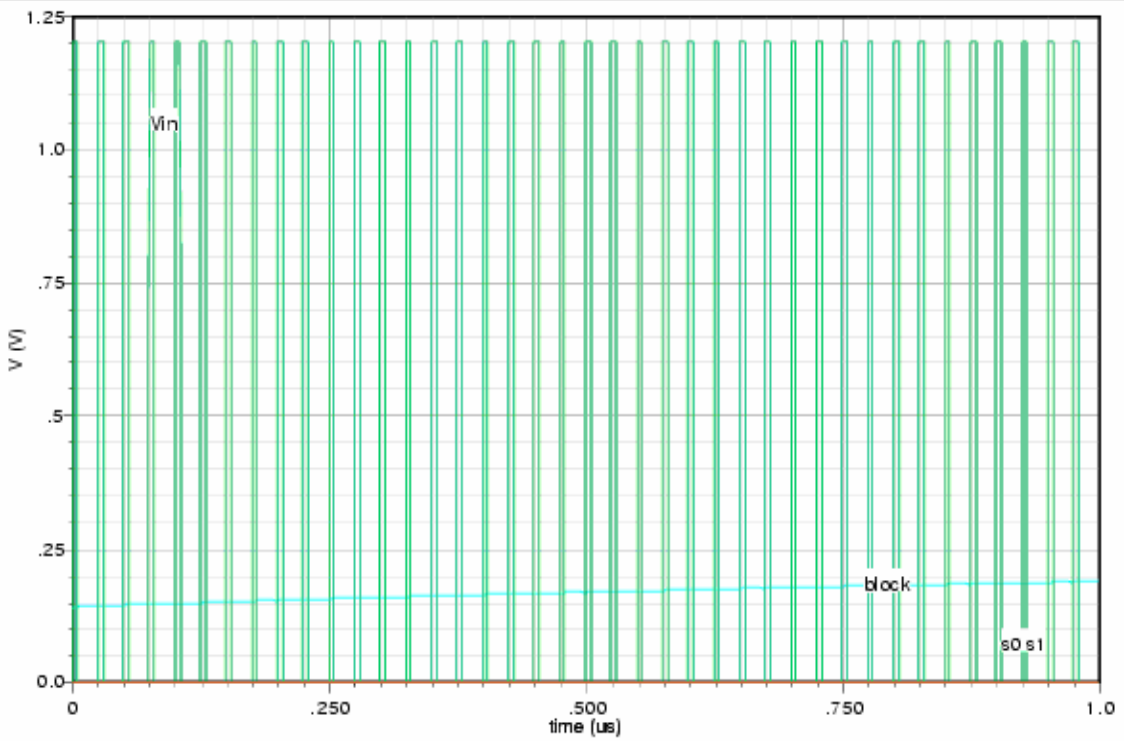


Output waveform for level down converter with Vddl = 1.02V, Vddh = 1.2V and load = 45fF.

Level blocking circuit

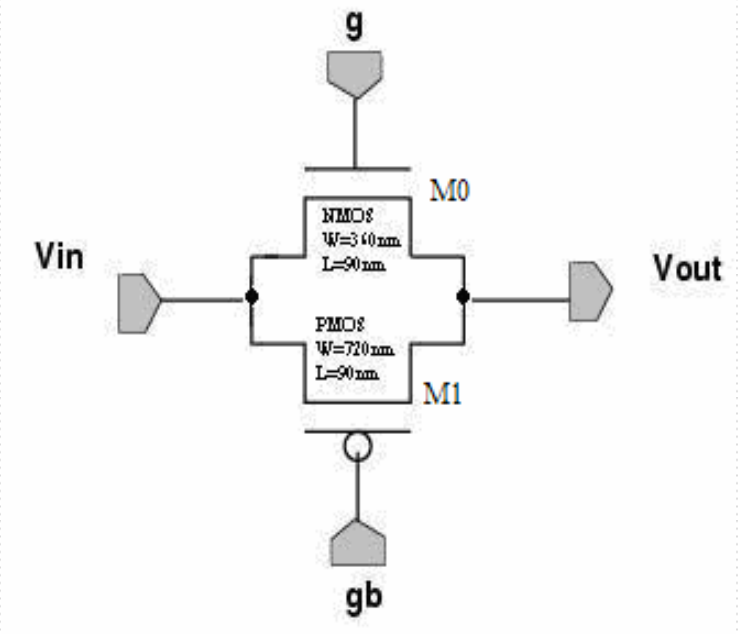


Transistor level circuit diagram of blocking circuit

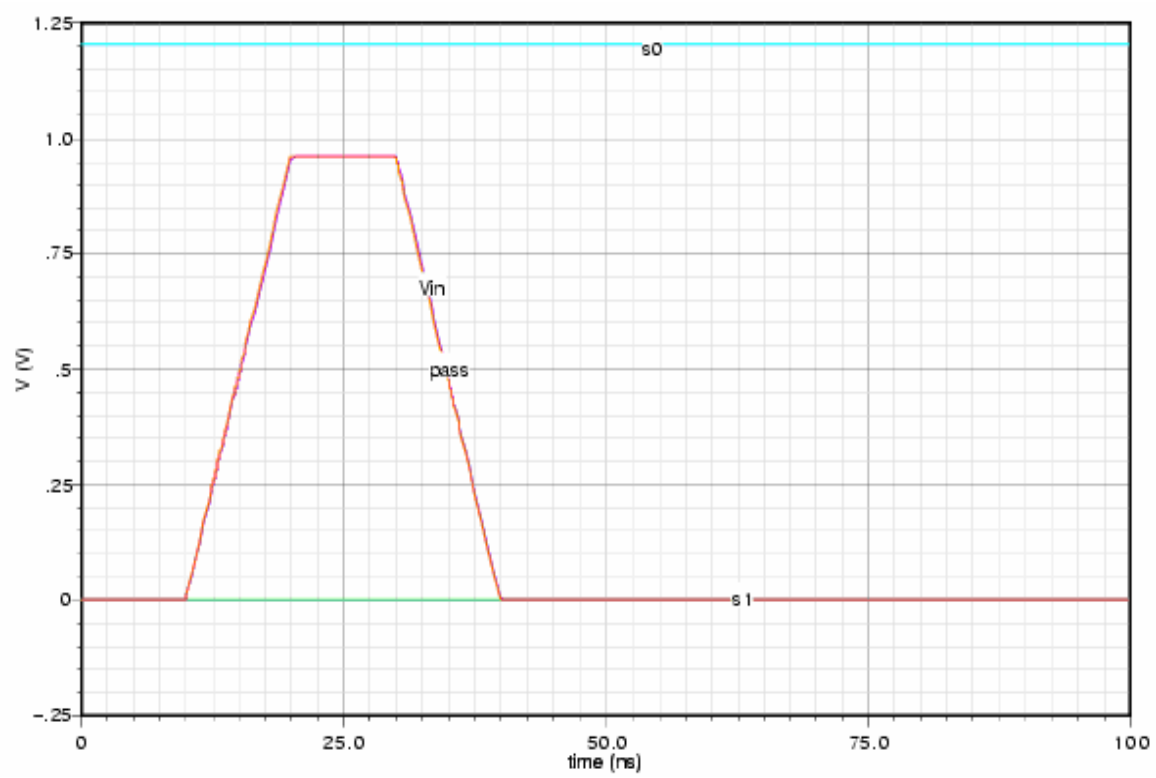


Output waveform for level up converter with Vddl = 1.02V, Vddh = 1.2V and load = 45fF.

Pass circuit



Transistor level circuit diagram of pass circuit

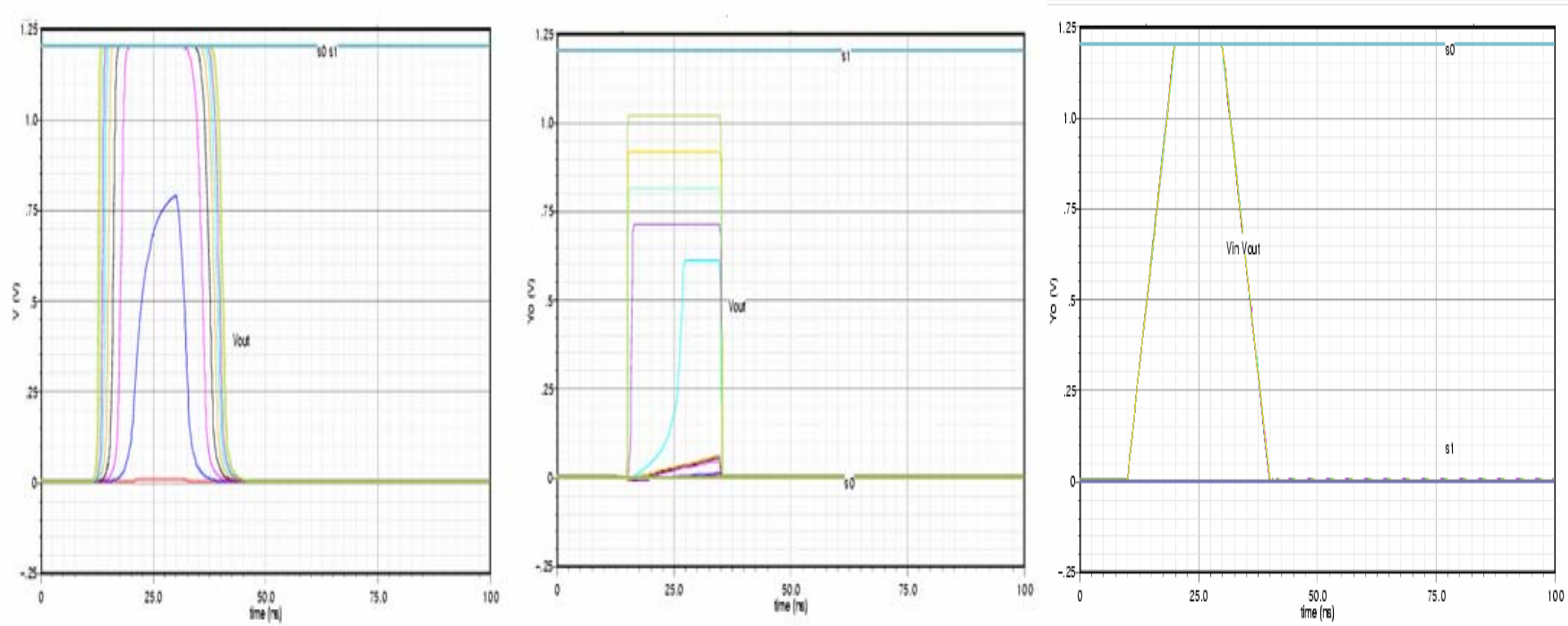


Output waveform for pass circuit with Vddl = 1.02V, Vddh = 1.2V and load = 45fF.

Characterization of ULC

- Parametric analysis
- Power analysis
- Load analysis

Parametric analysis

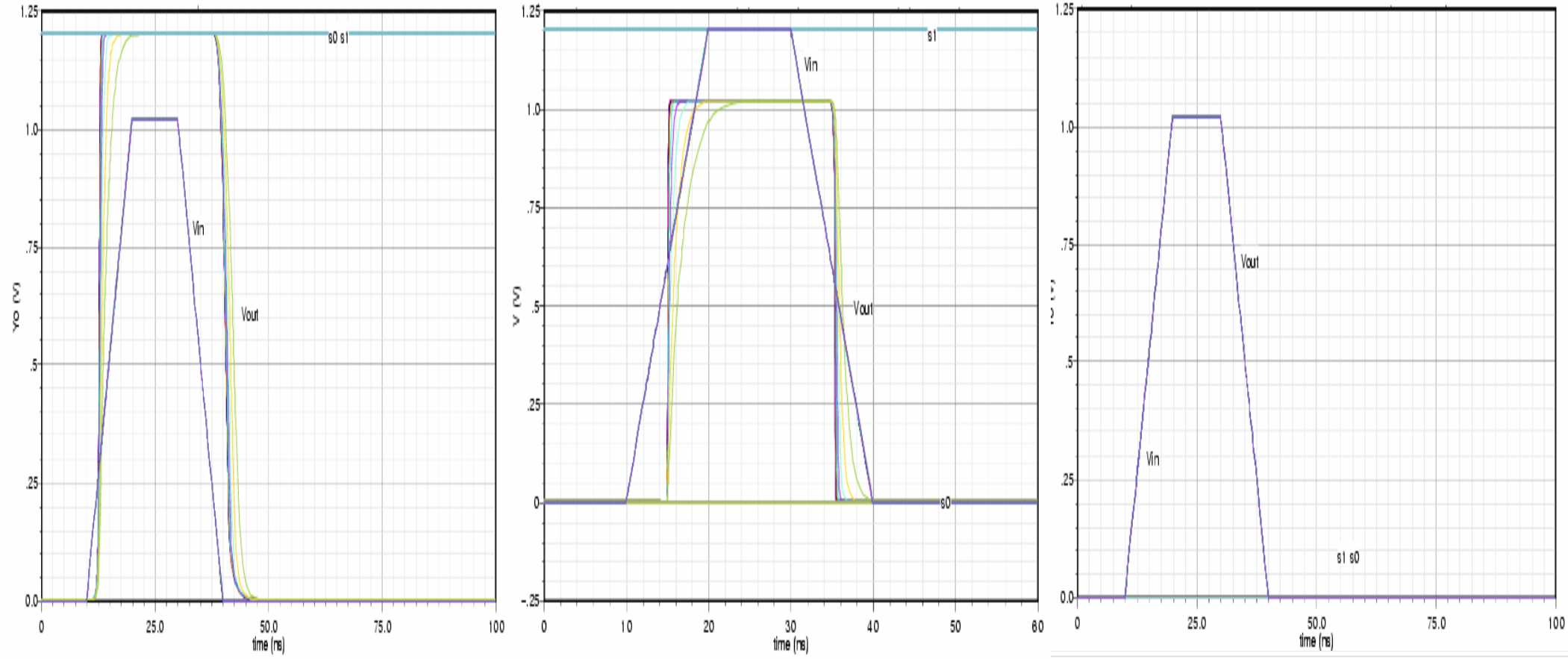


Output waveforms of parametric analysis of ULC where Vddl is varied from 0.1V to 1.02V and Vddh is kept constant at 1.2V

Power analysis

- Total average power of ULC = 26.928µW

Load analysis

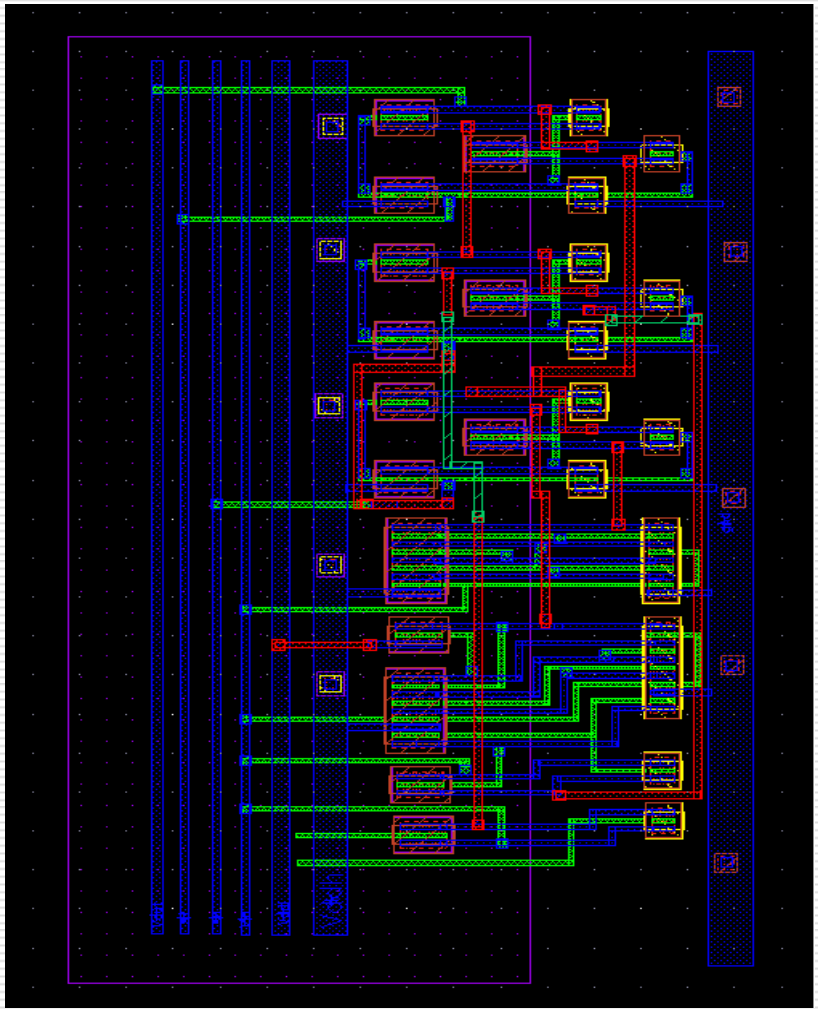


Output waveforms of load analysis of ULC where load is varied from 1fF to 200fF.

Custom layout design of ULC

- Layout design of ULC is created at 90nm technology
- PMOS W=1µm and L= 100nm
- NMOS W= 500nm and L= 100nm
- 90nm general process design kit
- Verified using the assuraDRC.rul during DRC check

Universal level converter



Conclusion

- Proposed a unique level converter design capable of four level converting operations
- Characterized the proposed design using parametric, power and load analysis at 90nm technology
- ULC consumes has an average power reduction of about 85-97% and is capable of producing stable output even under varying load from 1fF -200fF and at voltages as low as 0.6V

Future works

- Proposed design can be improved at schematic as well as layout level. Post layout simulation results to be presented.
- The technology can be further scaled down to 45nm.
- ULC design could be improved in the delay aspect.