Impact of Gate Leakage on Mixed Signal Design and Simulation of Nano-CMOS Circuits

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Outline of the Talk

- Introduction
- Related works
- Contributions of this paper
- Analog vs Mixed signal
- Design : Analog vs Mixed signal
- Simulation results
- Mixed signal analysis on VCO and frequency divider : Observations
- Mixed signal analysis on VCO and frequency divider : Discrepancy Quantification
- Mixed signal analysis on VCO and frequency divider : Discrepancy Remedy
- Conclusions

Introduction

- Characterization of mixed signal circuits using a 45*nm* CMOS Voltage controlled oscillator with frequency divider as base line circuit.
- Analog and digital blocks in the circuit are simulated.
- Accuracy issues due to analog and digital simulation engines are discussed.
- The impact of gate leakage on device performance is modeled as “effective tunneling capacitance”.
- Tunneling capacitance allows accurate modeling and simulation of digital blocks with almost analog accuracy.

Related Works
(Phase Locked Loops)

- B. Razavi 1996- Monolithic Phase-Locked-Loops and Clock Recovery Circuits.
- C. Xu, W. Sargeant, K. R. Laker, and J. vander Spiegel 2002- High performance VCO design using analog feedback control.
- P. Larsson 1999- Low power PLL design by reducing V_{DD}.
- J. H. C. Zhan, J. S. Duster, and K. T. Kornegay 2004-NMOS VCO vs PMOS VCO.
- J. McNeill 1997-Jitter in Ring Oscillators.

Related Works
(Gate Leakage)

- A. J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout 2005- Gate leakage and decreasing supply voltage.
- V. Mukherjee, S. P. Mohanty, and E. Kougianos 2005- Dual Dielectric approach for gate tunneling reduction.
- K. Narashimhulu and V. R. Rao 2006-performance analysis of common source amplifiers and current mirrors.
- S. P. Mohanty, R. Velagapudi, and E. Kougianos 2006- Dual-K vs Dual-T technique for gate leakage reduction.

Contributions of this paper

- A 45*nm* VCO was designed (analog). A frequency divider was designed (analog and digital).
- The analog and digital simulations of the frequency divider were compared.
- The effect of gate leakage on operation of frequency divider is quantized as “effective tunneling capacitance”.
- This effect is incorporated in the digital behavioral simulations of the frequency divider.
- Quantitative measures of the relative magnitude of gate leakage versus traditional gate capacitive effects on system operation are provided.

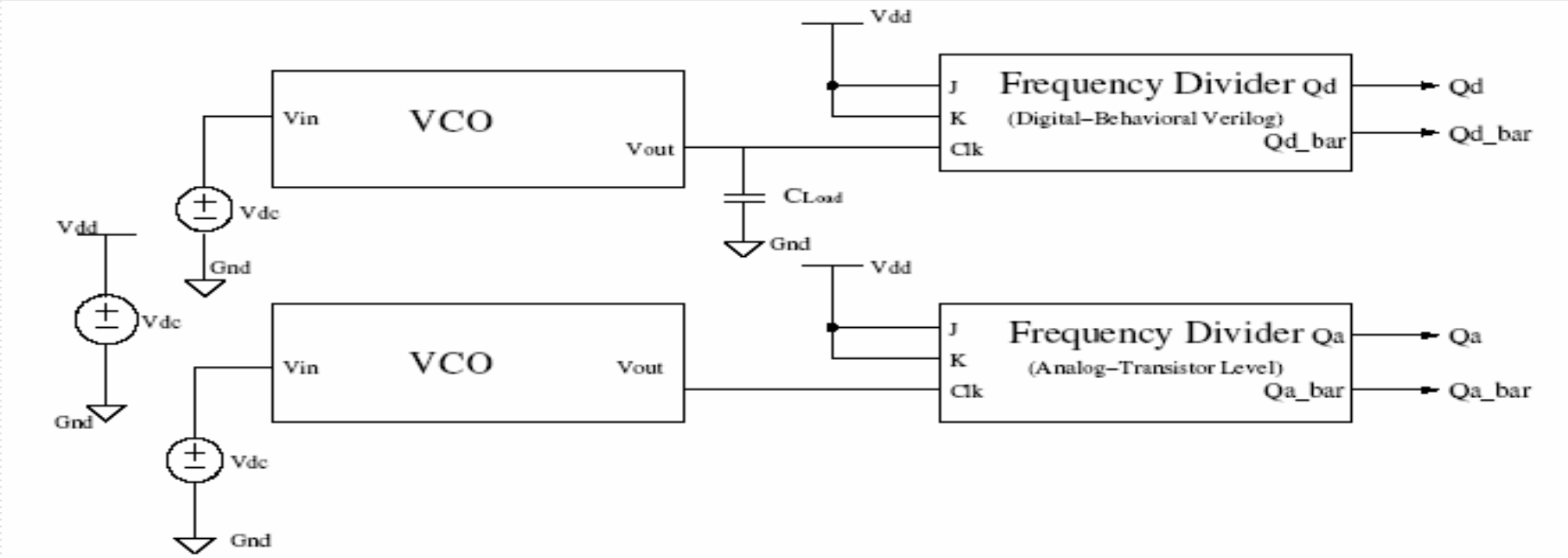
Analog vs Mixed signal

- Digital circuits more adaptable to technology scaling, but high precision processing requires analog circuits.
- Analog simulation results are superior but time consuming.
- Compromise in the form of mixed signal circuits.
- Metrics for analog and digital circuits are different. Hence mixed signal design is challenging.
- Mixed signal design is beneficial for low power, higher frequency of operation, smaller area.

Design : Analog vs Mixed signal

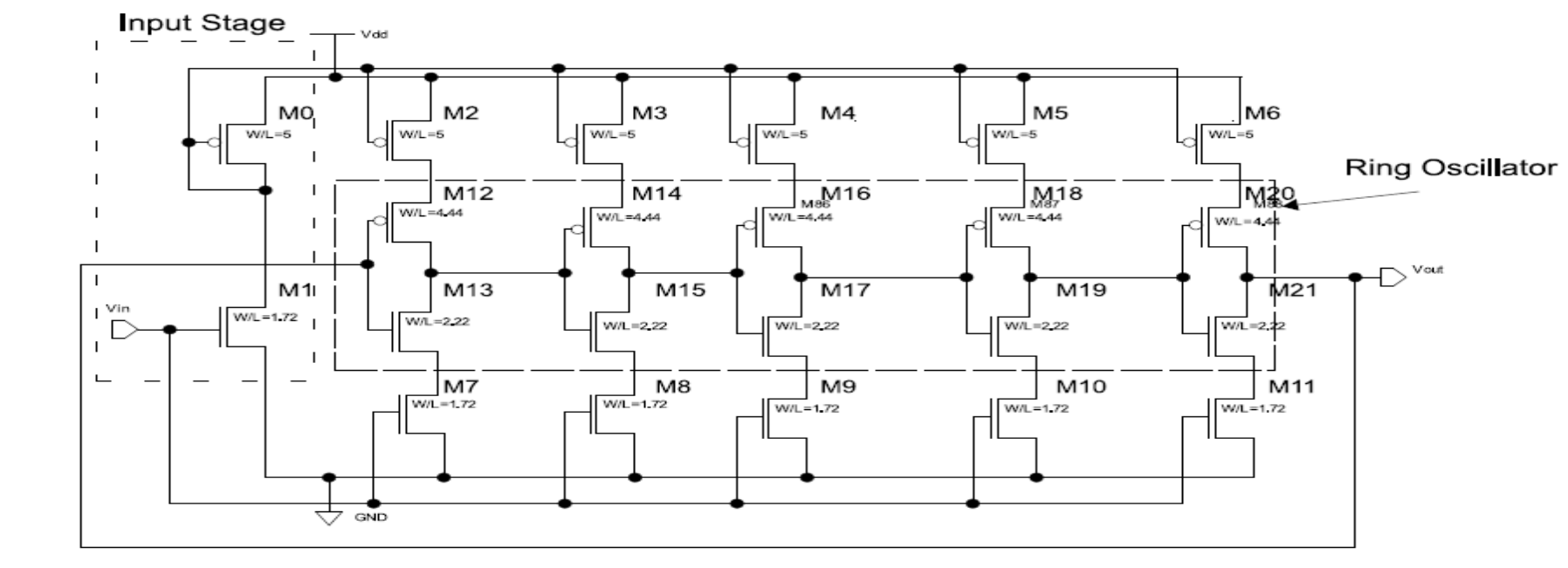
- Frequency from the VCO is changed using divide by ratio of the frequency divider.
- Case 1: analog VCO + analog frequency divider (transistor implementation).
- Case 2: analog VCO + digital frequency divider (modeled using behavioral level verilog).

Design : Analog vs Mixed signal



- Digital frequency divider vs analog frequency divider.
- Load capacitance added before digital frequency divider to model capacitive loading effects.

Design of analog VCO



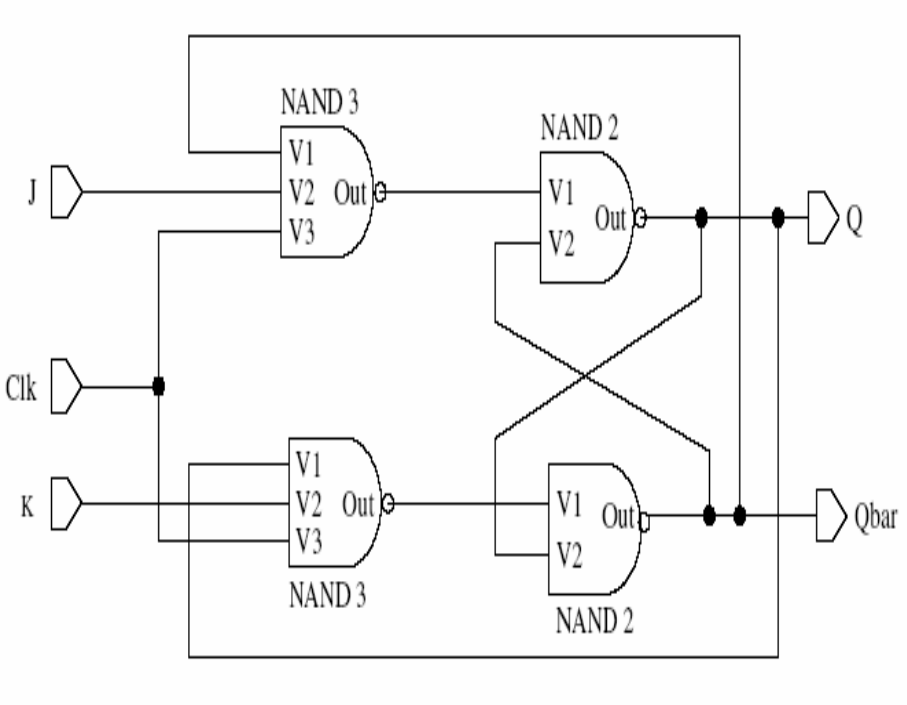
- Current Starved VCO
- Chosen keeping in mind the frequency performance.
- Other designs require large resistors and capacitors consuming a lot of area.

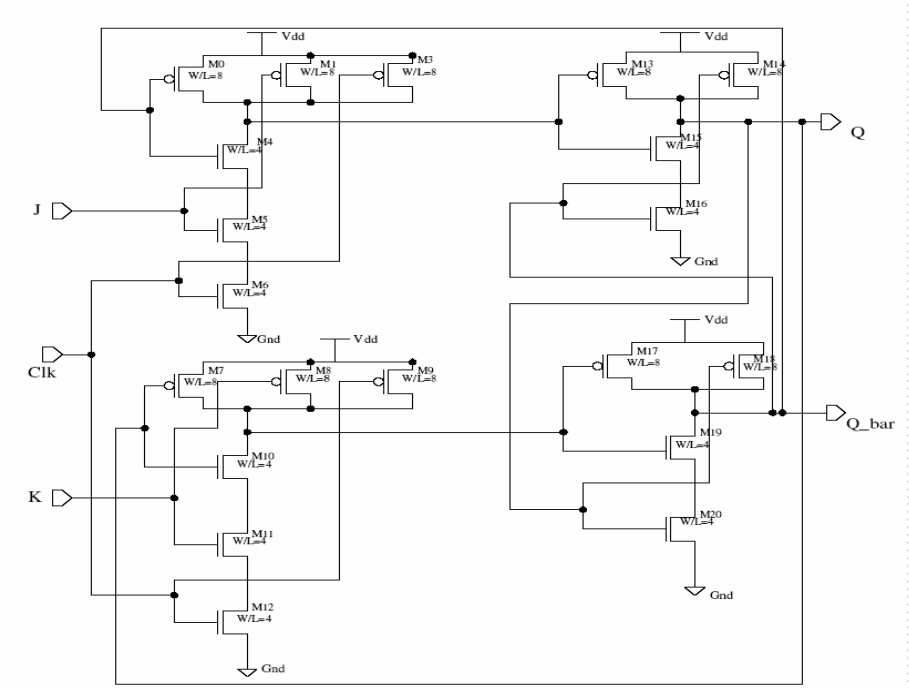
Current starved VCO

- Current Starved VCO comprises of
  - Odd numbered chain of inverters
  - Two input stage transistors => limit current flow to the inverter

- Frequency of oscillation (f_o) depends on
  - Number of inverters (N)
  - Size of the transistor (W/L)
  - Current flowing through the inverter (I_{inv}) which is dependent on the input voltage (V_{dd})
  - So, $f_o = I_{inv} / (N*C_{TOT}*V_{dd})$; where C_{TOT} is the total capacitance of the inverter transistors

Design of analog frequency divider





- JK flip flop: realized using two 3-input and two 2-input NAND gates.
- Output signal has approximately half the frequency of the input signal.

VCO Equations

Frequency of Oscillation

$$f_o = \frac{1}{N(T_{TOT})} = \frac{I_{inv}}{(N * C_{TOT} * V_{dd})}$$

where

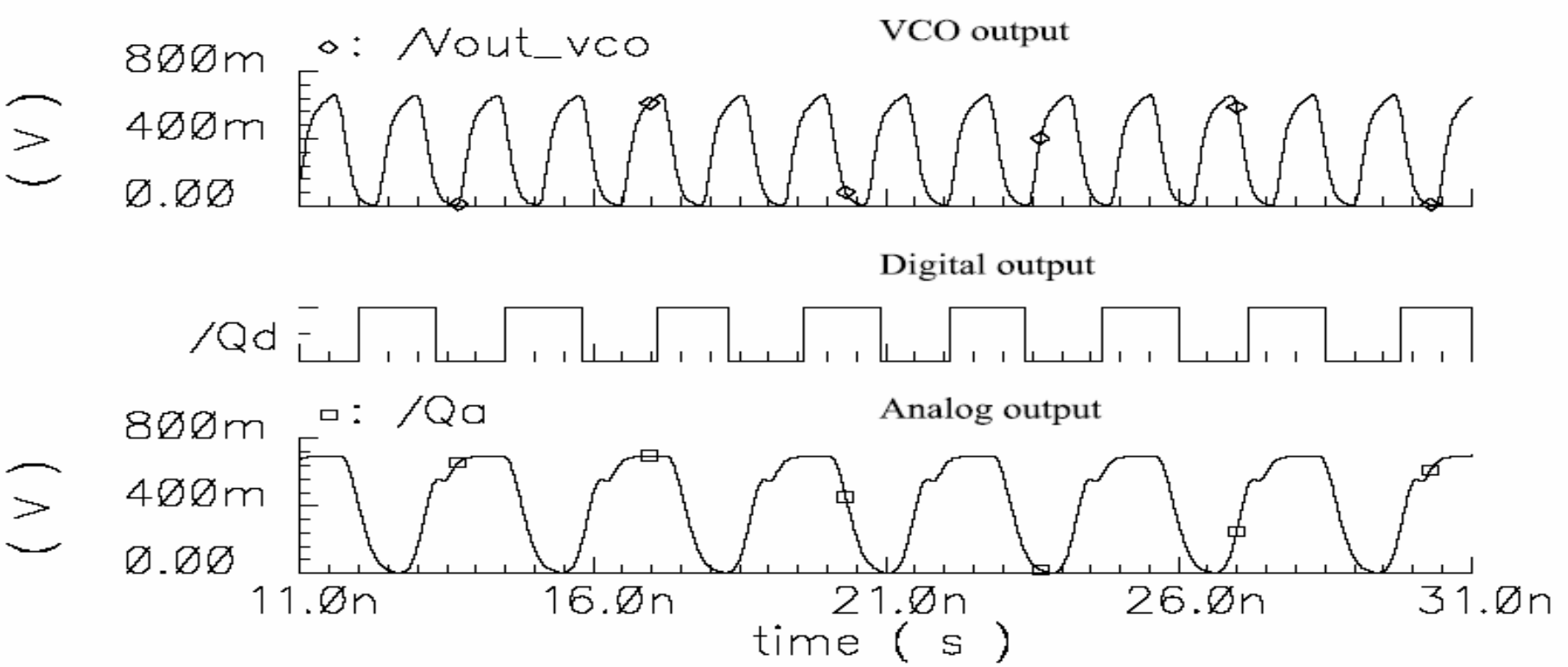
$$T_{TOT} = \frac{(C_{TOT} * V_{dd})}{I_{inv}}$$

and

$$C_{TOT} = C_O + C_I = \hat{C}_{ox}(W_p L_p + W_n L_n) + \frac{3}{2}\hat{C}_{ox}(W_p L_p + W_n L_n),$$

$$C_{TOT} = \frac{5}{2}\hat{C}_{ox}(W_p L_p + W_n L_n)$$

Simulation results



- Output waveforms of VCO, digital and analog frequency divider.
- f_{vco}=717.96 MHz, f_a=357.90 MHz and f_d=394.03 MHz.

Mixed Signal Analysis on VCO and Frequency Divider: Observations

- VCO – Analog design => Transistor level implementation.
- Frequency divider – Digital design => Behavioral Verilog code implementation.
- Frequency divider – Analog design => Transistor level implementation.
- Frequency of operation:
  - For VCO, f_{VCO} = 717.96 MHz
  - For analog frequency divider, f_a = 357.90 MHz
  - For digital frequency divider, f_d = 394.03 MHz
  - We have $\Delta f = |f_d - f_a| = 36.13 MHz$
- This frequency discrepancy is quite large (approx. 10 %) .

Mixed Signal Analysis on VCO and Frequency Divider: Discrepancy Quantification

- Gate leakage current is present during both ON and OFF states of a transistor.
- Effective tunneling capacitance:

$$C_{eff}^{tun} = \left| \frac{I_{ON} - I_{OFF}}{dv_g / dt} \right| dt = \frac{1}{T} \int_0^T \left| \frac{ig(t)}{dv_g / dt} \right| dt$$

V_g is the voltage applied on the gate.

- Calculation yields a value of 2fF. To minimize error within 1 %, we use C_{LOAD}=2.49fF.
- $C_{LOAD} = C_{Tunneling} + C_{Gate}$. However 80% of the capacitive load is due to gate tunneling. 20% is due to traditional gate capacitance.

Mixed Signal Analysis on VCO and Frequency Divider: Discrepancy Remedy

- Gate leakage phenomenon must be considered when operating at nano-scale technologies, particularly below 45*nm*.
- The difference in frequencies can be removed by adding a capacitor C_{LOAD} of 2.49 fF of which 2 fF is due to gate tunneling and 0.49 fF is due to capacitive loading.
- The gate tunneling capacitance is calculated as:

$$C_{eff}^{tun} = \left| \frac{I_{ON} - I_{OFF}}{dv_g / dt} \right| dt = 2.0\ fF$$

Conclusions

- Comparison of purely analog and mixed signal simulations at has been performed.
- 45*nm* VCO and frequency divider has been designed.
- Degradation in the performance is observed due to gate tunneling
- This degradation is equalized using a capacitive load before the digital block.
- The value of this capacitance is determined by leakage considerations and not traditional gate capacitance.
- This effect is more dominant in technologies 45*nm* and less.