A 45*nm* Flash Analog to Digital Converter for Low Voltage High Speed System-on-Chips

Dhruva Ghai, Saraju P. Mohanty and Elias Kougianos
VLSI Design and CAD Laboratory (www.vdcl.cse.unt.edu)
Dept. of Computer Science and Engineering
University of North Texas
dvg0010@unt.edu, smohanty@cse.unt.edu, eliask@unt.edu

Presented by Dhruva Ghai
University of North Texas
dhruva@unt.edu

Outline

- Introduction and Motivation
- Specifications
- Related Research Works
- Design of flash ADC
- The TIQ principle
- TIQ Comparator
- Sizing of transistors
- Functional Simulation
- Ideal vs Actual Characteristics
- DNL
- INL
- SNDR
- Instantaneous Power Plot
- Conclusion and Future Works

Introduction and Motivation

- ADCs are interfaced with digital circuits in mixed signal chips, where digital signal processing is performed.
- Supply voltage decreasing rapidly for digital circuits as technology scales.
- Analog to digital converters required to be operating with these devices at the same voltages.
- The proposed design meets both criteria: Low supply voltage ($0.7V$) and technology ($45nm$).

Specifications

- Resolution : 6 bits.
- Technology : 45*nm*.
- Speed : 1*Gs/sec*.
- V_{LSB} : 500μV.
- V_{DD} : 0.7*V*.
- INL : 0.46*LSB*.
- DNL : 0.70*LSB*.
- SNDR : 31.9*dB*.

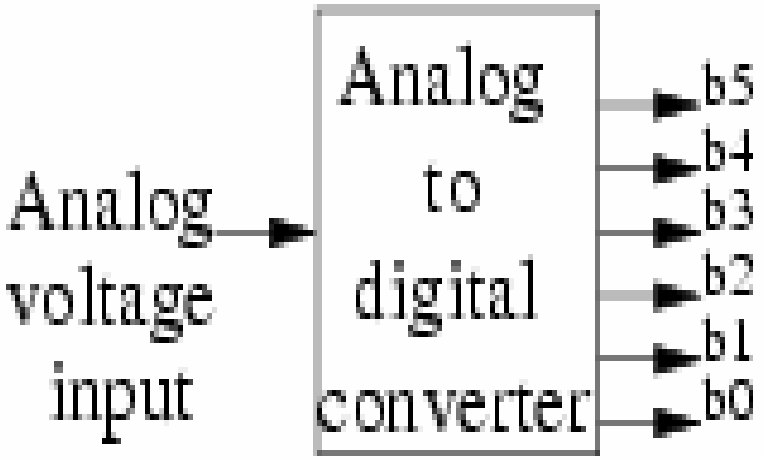
Related Research Works

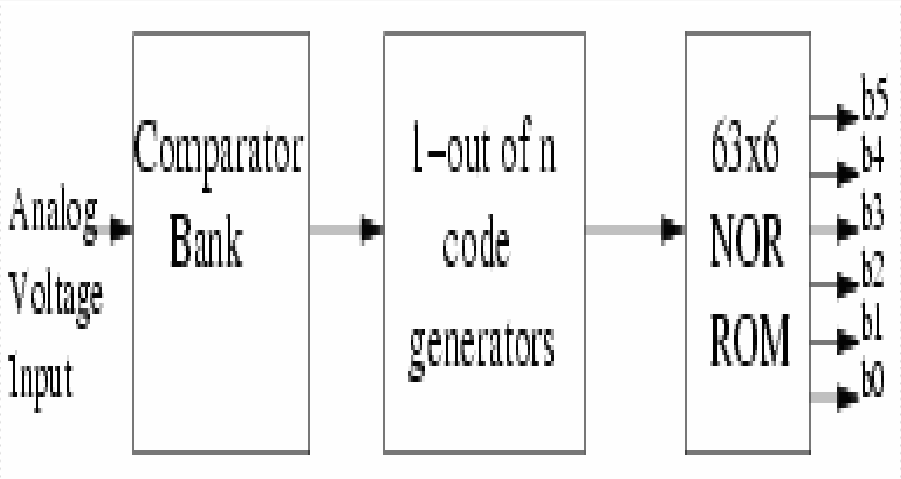
Reference	Resolution (bits)	Technology (nm)	DNL (LSB)	INL (LSB)	SNDR (dB)	VDD (V)	Power (mW)	Samples/sec.
Choi 2001	6	350	<±0.3	<±0.3	32	3.3	545	1.3G
Donovan 2002	6	250	-----	-----	33	2.2	150	400M
Geelen 2001	6	350	<0.7	<0.7	5.6 (ENOB)	3.3	300	1.1G
Lee 2002	6	250	1.04	0.81	-----	2.5	59.91	1.11G
Mehr 1999	6	350	<0.32	<0.2	>5(ENOB)	3.3	225	500M
Sandner 2005	6	130	<0.4	<0.6	32.5	1.5	160	600M
Scholtens 2002	6	180	-----	0.42	5.7(ENOB)	1.95	328	1.6G

Related Research Works….

Reference	Resolution (bits)	Technology (nm)	DNL (LSB)	INL (LSB)	SNDR (dB)	VDD (V)	Power (mW)	Samples/sec.
Song 2000	6	350	-0.6	0.7	33.5	1	10	50M
Srinivas 2006	6	350	0.3	0.3	33.6	3.3	50	160M
Tseng 2004	6	250	<±0.1	<±0.4	32.7	2.5	35	300M
Uyttenhove 2000	6	350	-----	-----	32	3.3	-----	1G
Uyttenhove 2002	6	250	0.42	0.8	32	1.8	600	1.3G
Yoo 2001	6	250	-----	-----	-----	2.5	66.87	1G
This Work	**6**	**45**	**0.7**	**0.46**	**31.9**	**0.7**	**45.42µW**	**1G**

Design of flash ADC



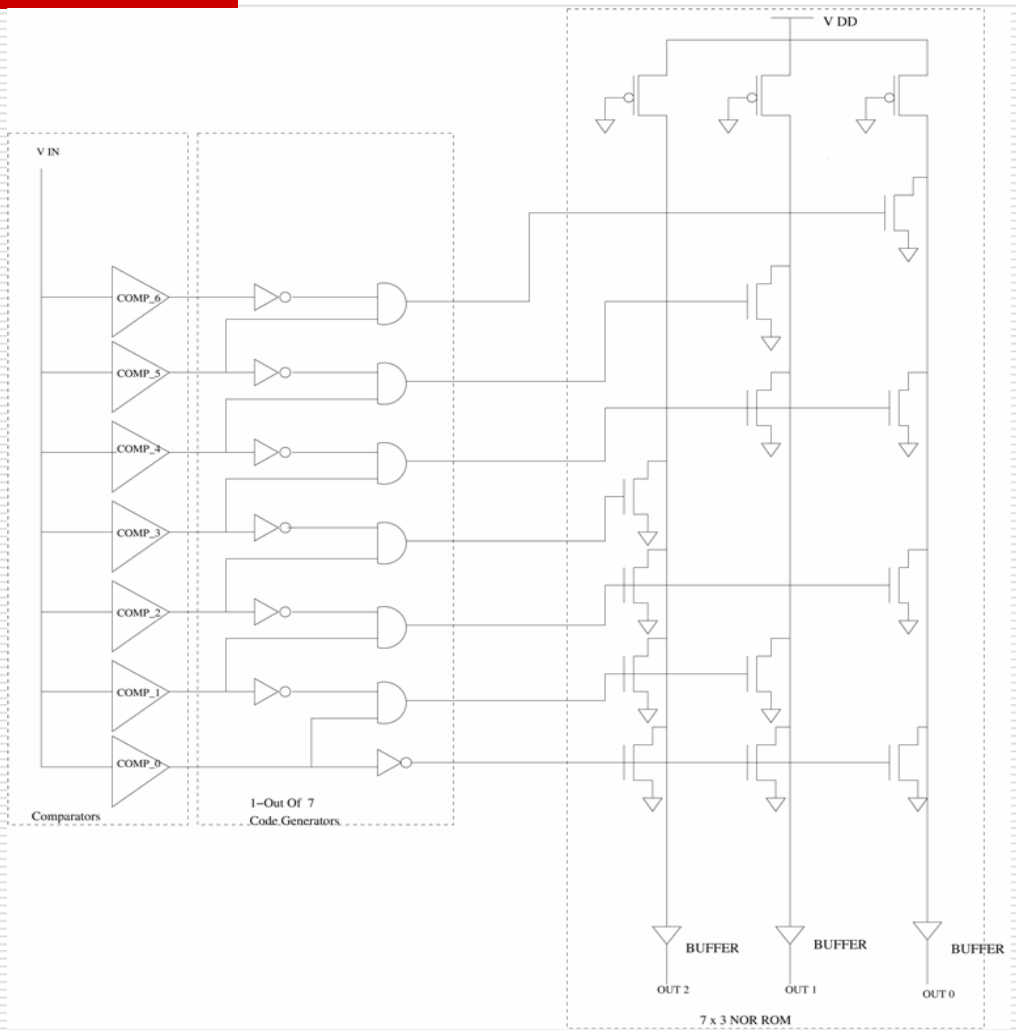


- High level block diagram of ADC.
- Input is analog (generally ramp or sine wave).

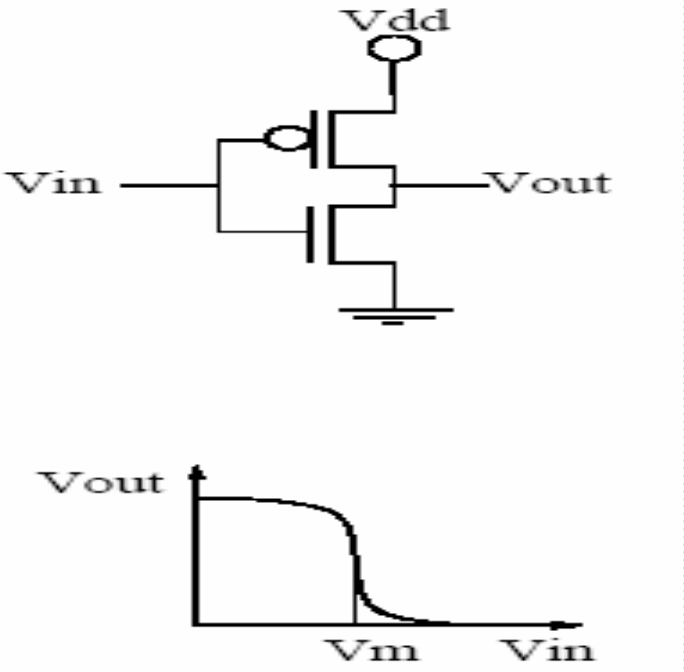
- Output of Comparator Bank is thermometer code.
- Converted to 1-out of n code using 1-out of n code generators.
- NOR ROM converts the 1-out of n code to binary code.

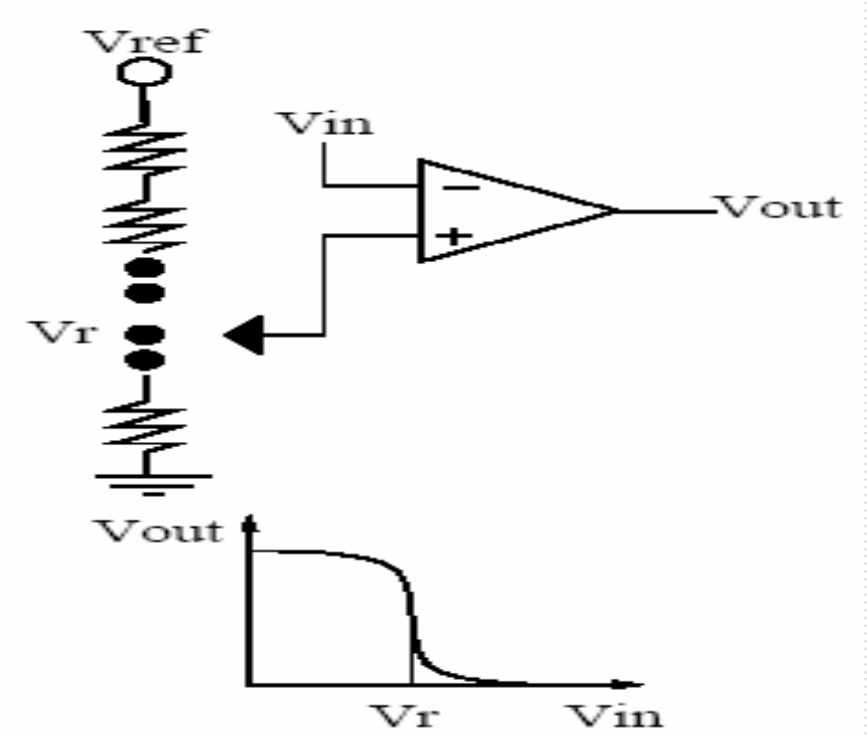
Design of flash ADC

- For an n-bit ADC we need: 2^n-1 Comparators.
- 1-out of n code generators.
- NOR ROM : 2^n-1 X n.
- For discussion purposes,3-bit flash ADC is shown. 6-bit ADC has similar structure.



Threshold Inverter Quantization Principle

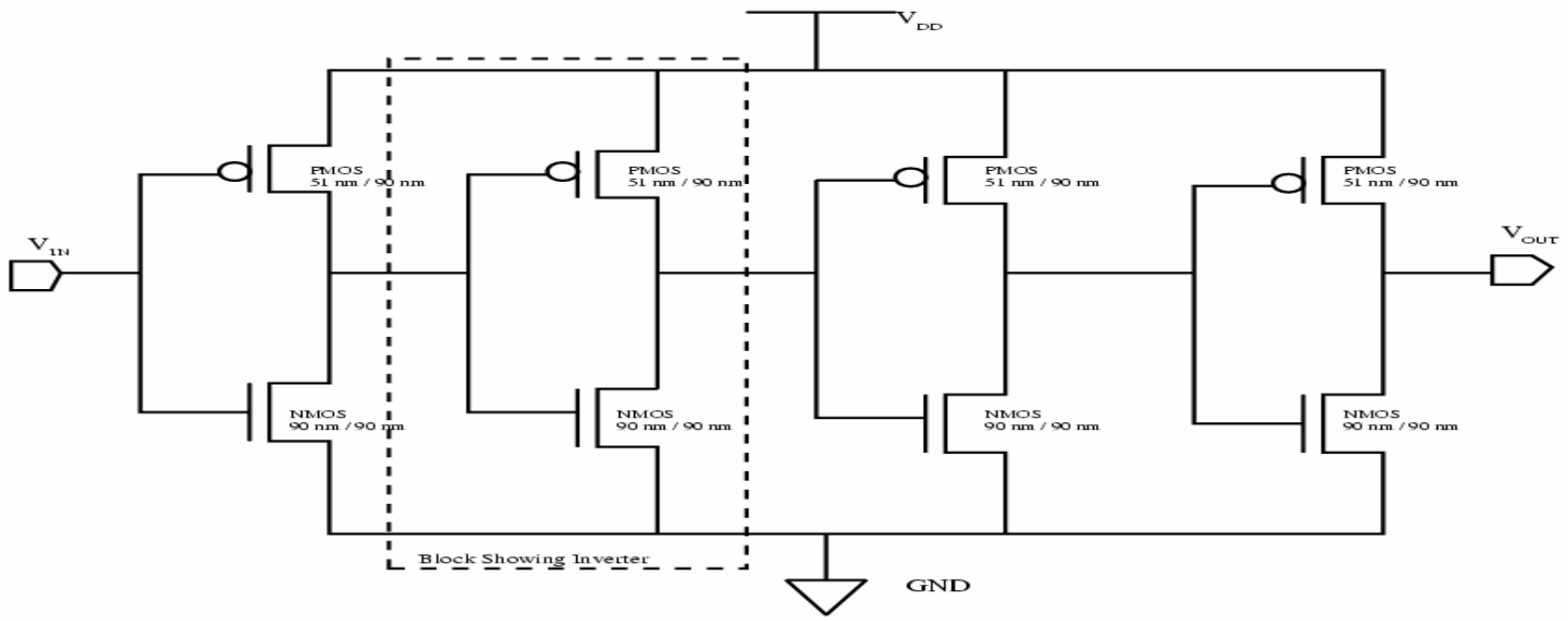




- TIQ comparator.
- Formed by cascading of digital inverters.
- Sizing of transistors determine switching point.

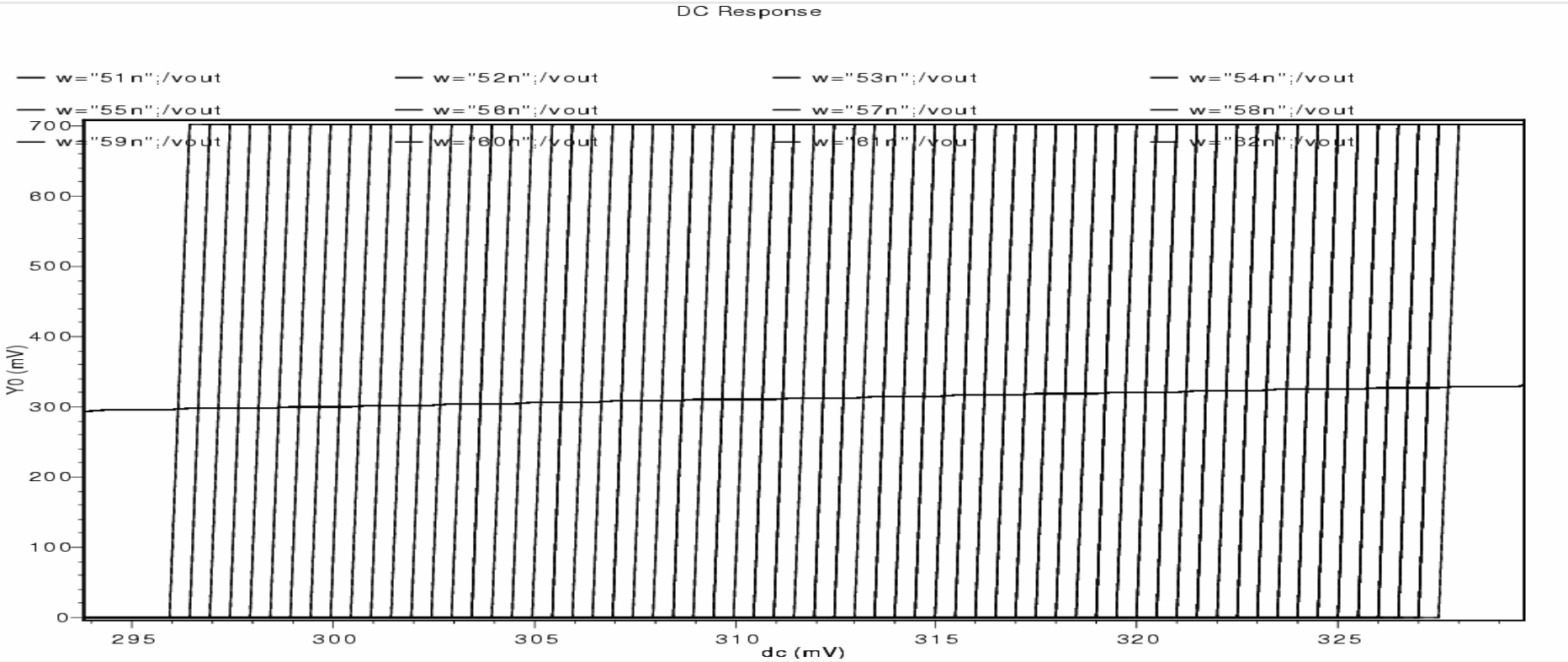
- Differential comparator.
- Require resistive ladder network.
- Area overhead increases.

TIQ Comparator



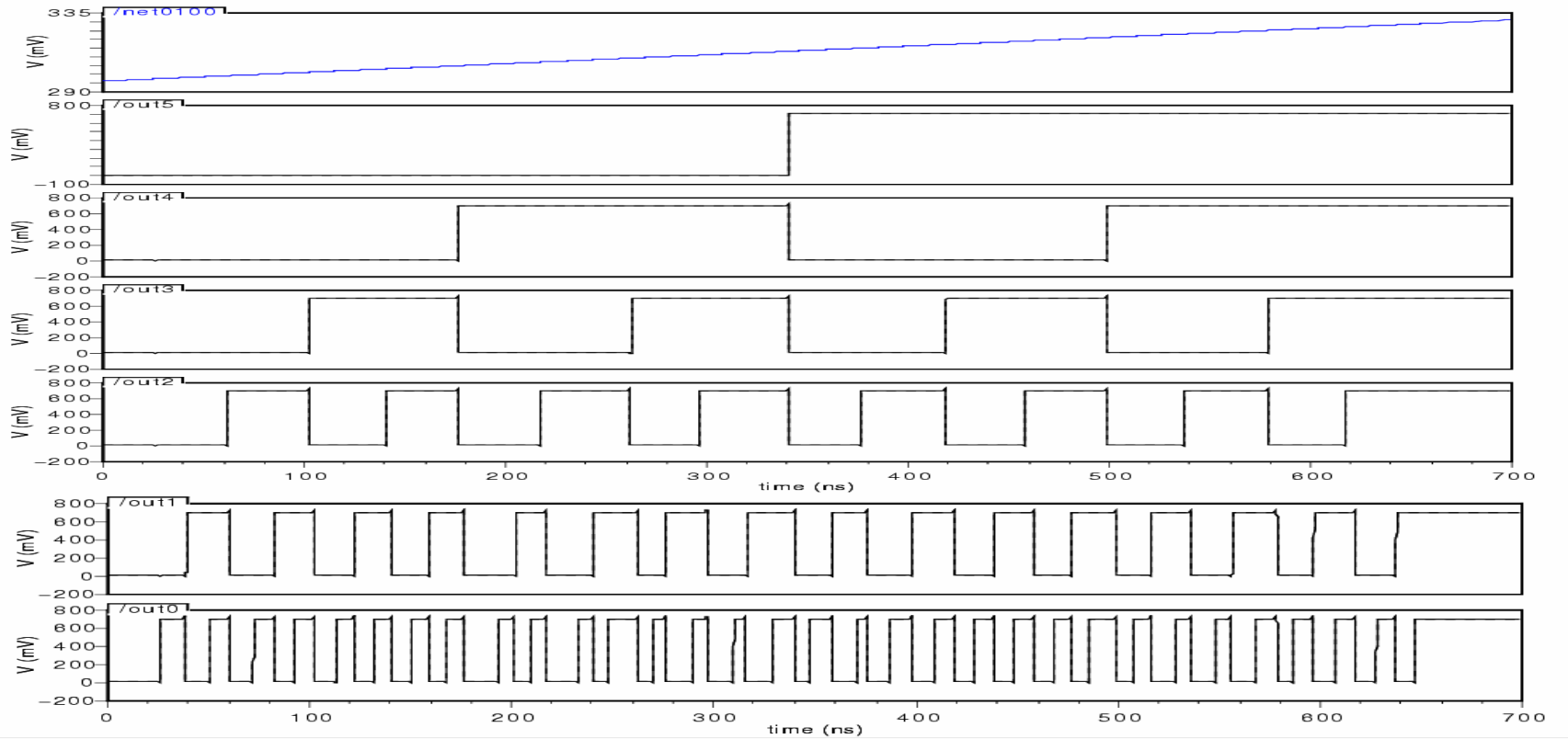
- Formed by four cascaded inverters.
- Provide a sharper switching for the comparator and full voltage swing.
- Sizes of PMOS and NMOS in a comparator are same, but different for different comparators.

Transistor sizing



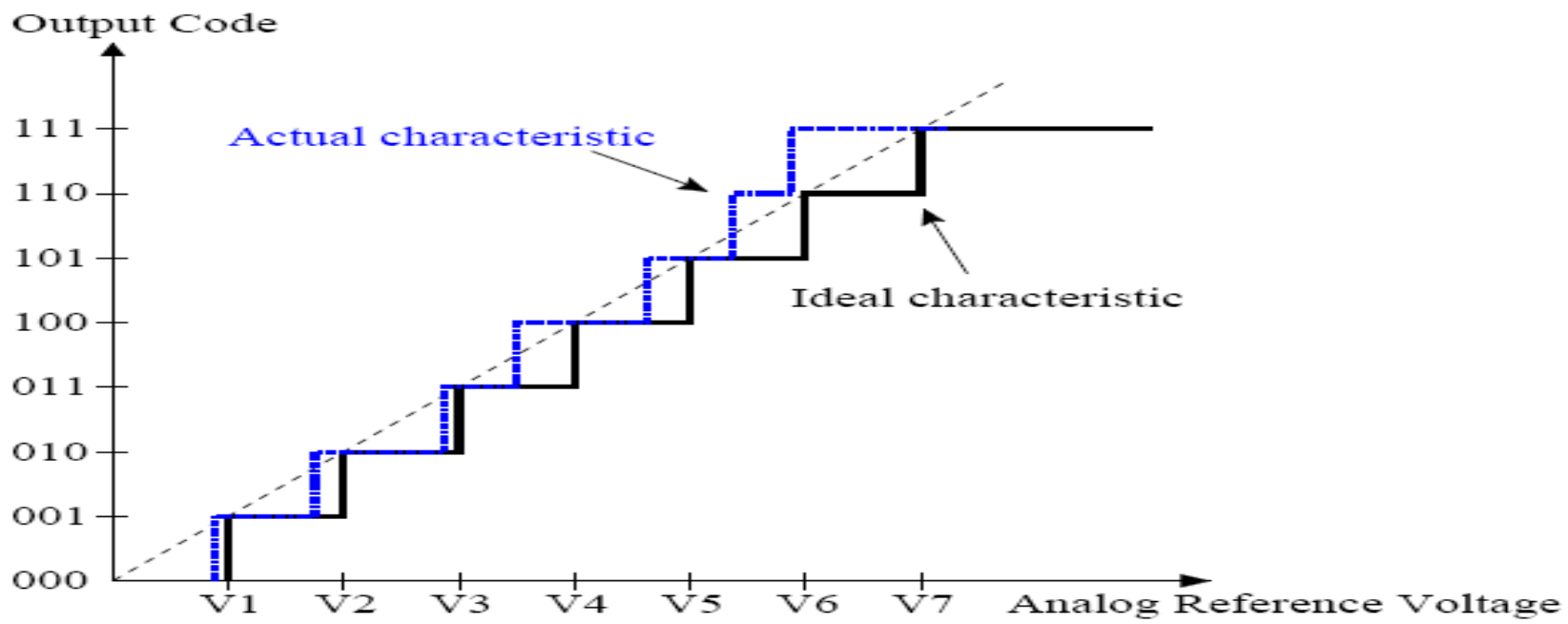
- DC parametric sweep is used to determine the transistor sizes.
- Input voltage varied from 0 to 0.7V in steps of 500μV.
- W/L for NMOS transistors kept as 90nm/90nm. L for PMOS transistors kept as 90nm. W for PMOS transistors was given a parametric sweep in steps of 1nm. Minimum width=51nm,maximum width=163nm.

Functional Simulation



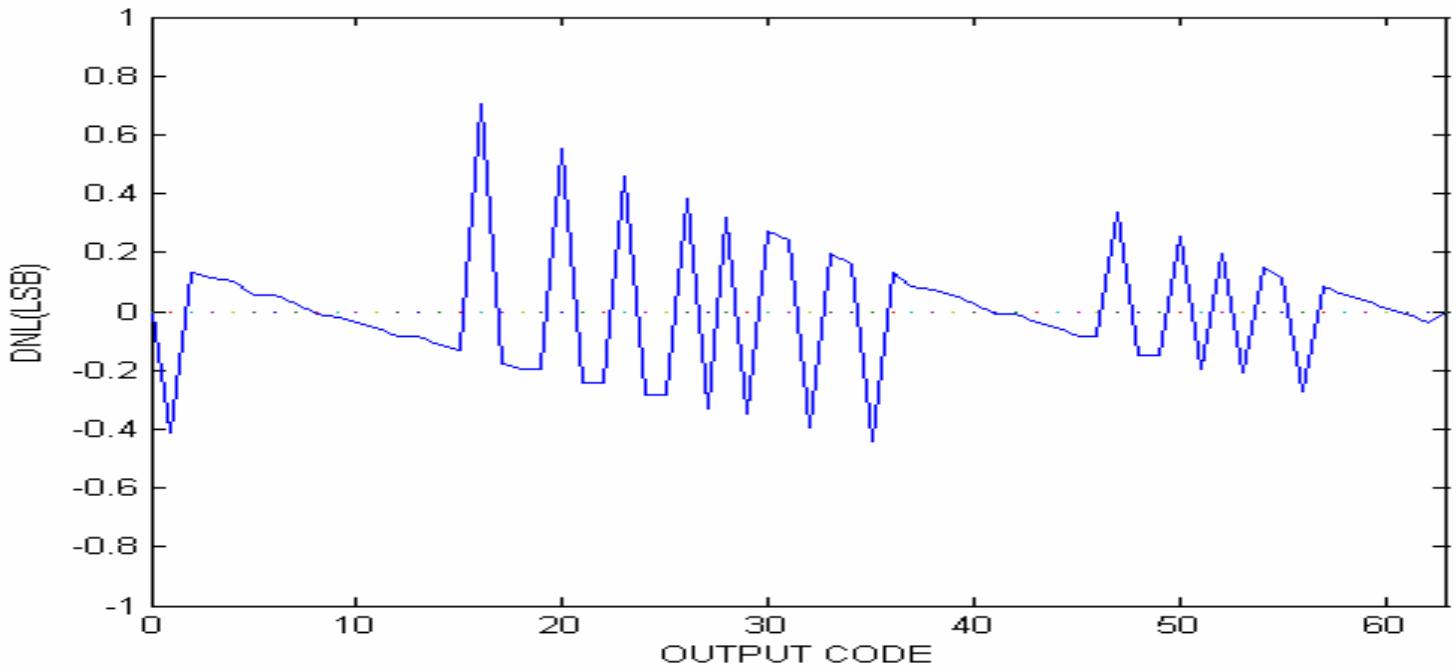
- Transient analysis carried out.
- Ramp generated from 296.3*mV* to 327.8*mV*. Digital codes going from 0 to 63 are obtained at the output.

Ideal vs Actual Characteristics



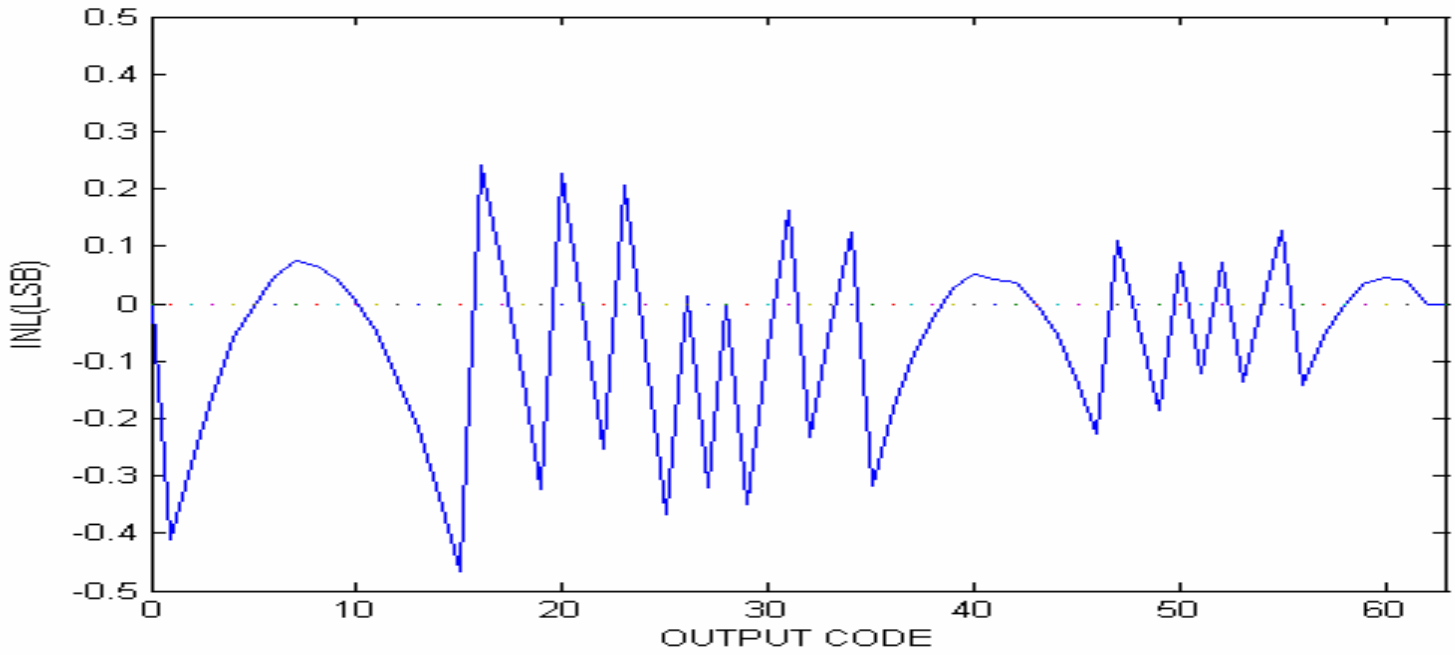
- Ideal vs actual transfer function
- Due to transistor implementation, actual transfer function never equal to ideal transfer function.
- Characterized using DNL and INL.

Max DNL of ADC = 0.7*LSB*



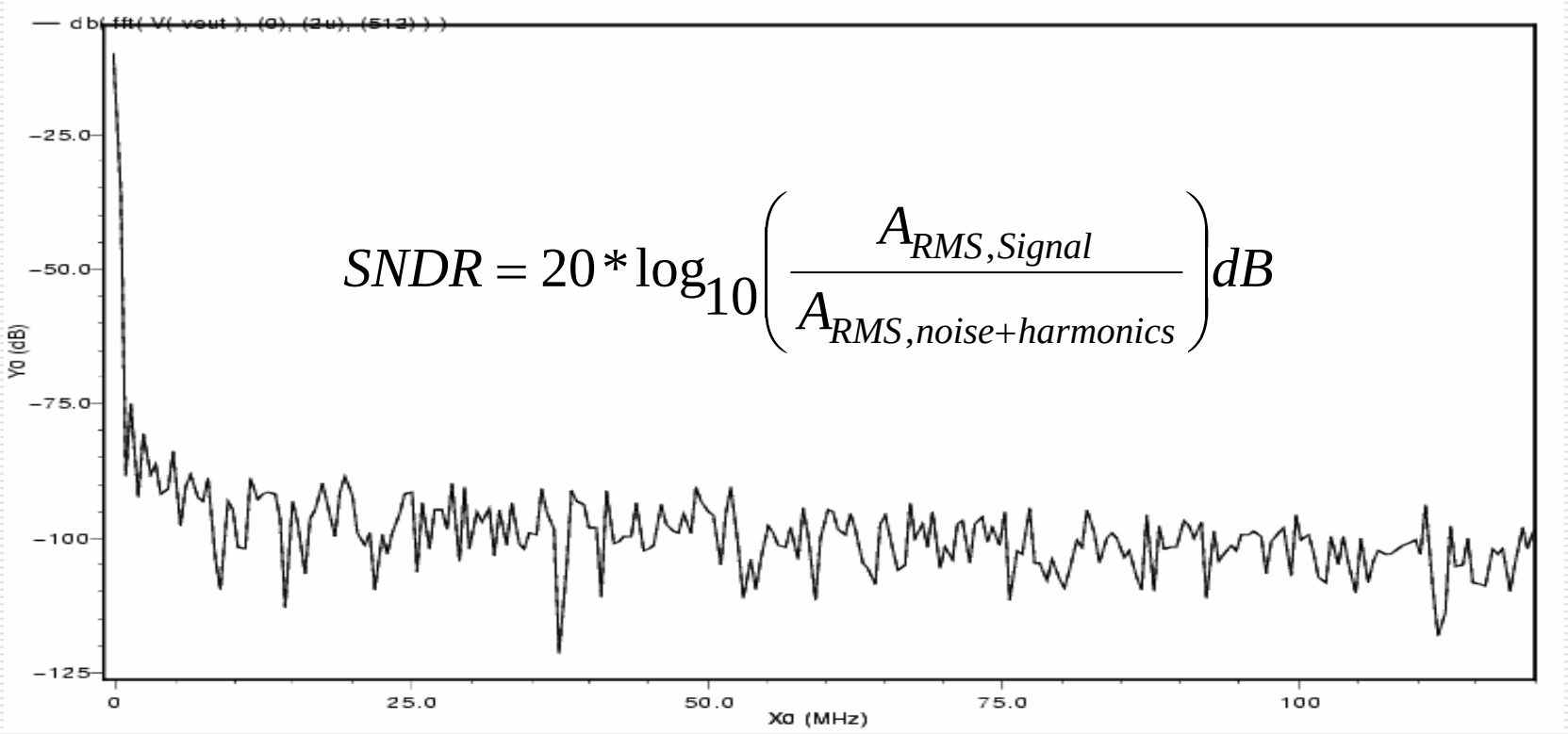
- Differential Non-Linearity. Difference between actual step width and ideal value of 1LSB.
- Modeled as Verilog-A block. Uses histogram method. DNL<1*LSB* ensures monotonicity.

Max INL of ADC =0.46*LSB*



- Integral No-linearity. Deviation of actual transfer function from a straight line. expressed in *LSB*.
- Verilog-A block used. Slowly varying ramp given as input, covering full scale range in 4096 steps.

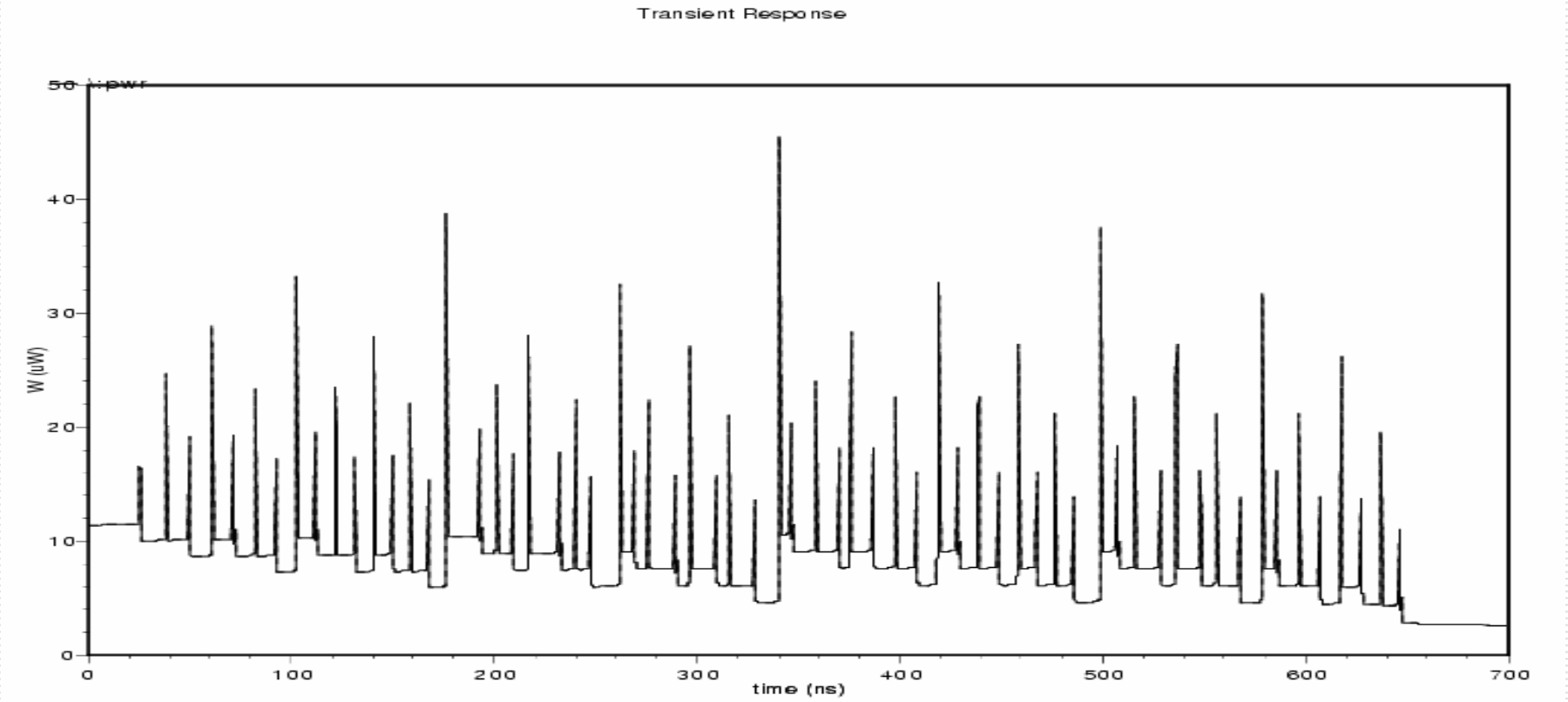
SNDR = 31.9*dB*



$$SNDR = 20 * \log_{10}\left(\frac{A_{RMS,Signal}}{A_{RMS,noise+harmonics}}\right) dB$$

- Signal to noise and distortion ratio.
- ADC output fed to Ideal DAC. FFT of DAC output obtained. SNDR calculated from this.

Instantaneous Power Plot



- Peak Power=45.42μW.
- Avg. Power=8.8μW.
- Low power design.

Conclusion and Future Works

- Successful ADC design at nano-scale (45*nm*)technology.
- DNL=0.7*LSB*,INL=0.46*LSB*.
- SNDR=31.9*dB*, Low power design (Avg. Power = 8.8μW).
- Layout using 90*nm* general process design kit.
- Scaling the layout rules to perform layout at 45*nm*.