Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation

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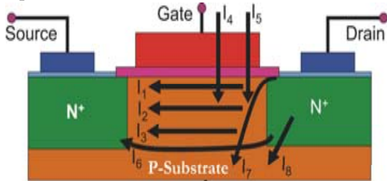
Abstract

- *To achieve power-performance trade-offs one varies different parameters: Tox, K, Vth, L, and VDD.*
- *If Tox, L, Vth, and VDD, etc. are scaled simultaneously, will one obtain a power and performance optimal circuit that has minimal gate leakage, minimal subthreshold leakage, and minimal dynamic power consumption?*
- Seven different cases, such as (1) only *Tox* scaling, (2) only *Vth* scaling, (3) only *VDD* scaling, (4) simultaneous *Tox* and *Vth* scaling, (5) simultaneous *Tox* and *VDD* scaling, (6) simultaneous *Vth* and *VDD*, and (7) simultaneous *Tox*, *Vth*, and *VDD* scaling, are analyzed for optimization.

Introduction

Current flow paths in a nano-CMOS transistor during power dissipation in different states of operation:



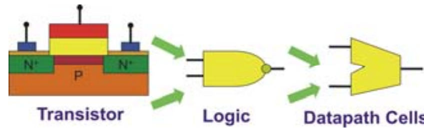
I_1: drain to source active current (ON state), I_2: drain to source short circuit current (ON state), I_3: subthreshold leakage current (OFF state), I_4: gate oxide leakage current (both ON and OFF states), I_5: gate current due to hot carrier injection (both ON and OFF states), I_6: channel punch through current (OFF state), I_7:gate-induced drain leakage (OFF state), and I_8: reverse bias PN junction leakage (both ON and OFF states).

3 Major Components of Total Power Dissipation

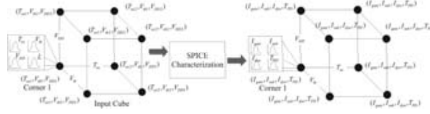
- Capacitive Switching Current
- Gate Oxide Leakage
- Sub-threshold Leakage

Process Variation Aware Power and Performance Characterization

A hierarchical methodology is followed to characterize architectural level units for gate leakage, subthreshold leakage, and dynamic power, as well as their propagation delay.



- The input process and design variations are assumed to be Gaussian in nature.
- Via Monte Carlo simulations, we translated the process and design variations (inputs) into gate leakage, dynamic and subthreshold current and delay probability density distributions (outputs).



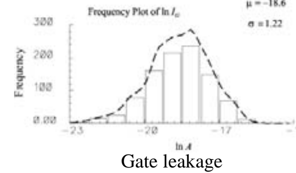
The functional units are synthesized into a network of 2-input NAND gates. Since the total current in the functional unit can be defined as the sum of currents in the individual NAND gates, and the distributions for each gate are statistically independent of each other, the mean and variance of the currents can be derived as:

$$\mu_{FU} = N * \mu_{NAND}$$
$$\sigma_{FU} = \sqrt{N} * \sigma_{NAND}$$

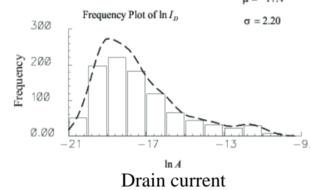
where there are N NAND gates in the implementation of the functional unit.

Accounting for Process Variation

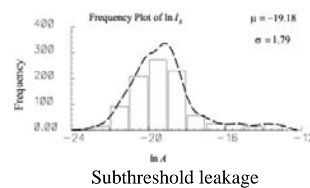
The provided statistical information for each input corner is used to generate N = 1000 Monte Carlo runs (per corner) which provides statistical distributions of the output parameter



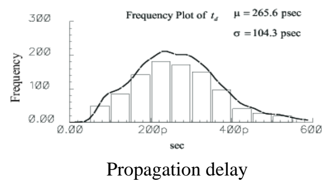
Gate leakage



Drain current



Subthreshold leakage

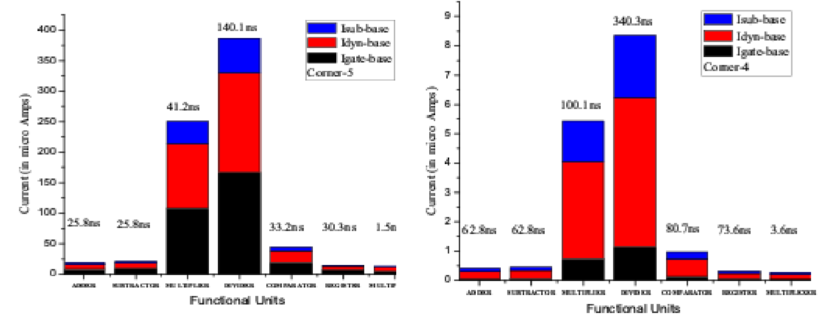


Propagation delay

Effects of statistical process variation on gate leakage, subthreshold leakage, dynamic power and propagation delay in a 2-input NAND gate.

Analysis of Effects of Scaling on Power Components

Characterization data for various corners:



Corner 5: *Tox* = 1.4nm, *Vth* = 0.22V, VDD = 0.9V   Corner 4: *Tox* = 1.7nm, *Vth* = 0.25V, *VDD* = 0.7V

Nominal results showing individual components of power consumption for different output corners. It may be noted that the total current values are reduced and the proportion of different components in the total current have changed. Only two corners are shown for brevity. In corner 5 *vs.* corner 4, all parameters have been scaled i.e. *Tox* and *Vth* are increased and *VDD* is decreased.

We refer to "scaling" as the process of reduction of power. In that sense, scaling *VDD* implies *reduction* in its value but scaling *Tox* and *Vth* implies an *increase* in their values.

Power Component	Parameter varied						
	T_{ox}	V_{th}	V_{DD}	$T_{ox}+V_{th}$	$T_{ox}+V_{DD}$	$V_{th}+V_{DD}$	$T_{ox}+V_{th}+V_{DD}$
Dynamic	88.3	52.6	70.1	94.3	93.4	73.5	96.8
Gate Leakage	96.2	11.3	69.2	97.7	98.8	72.7	99.3
Subthreshold Leakage	94.3	10.5	63.4	89.8	97.9	59.6	96.3
Total Current	91.6	46.1	57.8	94.8	96.4	71.1	97.8
Propagation Delay	65.8	17.0	21.4	100.0	101.4	42.1	142.9

Conclusions

- The effect of scaling of three parameters, *Tox*, *Vth*, and *VDD* on various power (current) components was studied.
- It was observed that simultaneous scaling of all three may not result in expected power-performance tradeoff, with the expectation derived simply from the effect of individual parameter variations.
- Hence, power optimization techniques in circuit or process design employing parameter selection or assignment need to do so judiciously based on multivariate effects.

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