A Comparative Analysis of Gate Leakage and Performance of High-K Nanoscale CMOS Logic Gates

Saraju P. Mohanty and Elias Kougianos
University of North Texas, Denton, TX 76203.
Email: smohanty@unt.edu and eliask@unt.edu

Rabi N. Mahapatra
Texas A&M University, College Station, TX 77843.
Email: rabi@cs.tamu.edu

Abstract

Replacement of SiO2 as gate dielectric with alternative high-K dielectric materials, is considered as a method to contain the gate leakage current.

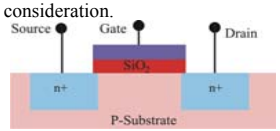
This paper provides novel attempts to evaluate the gate leakage current and propagation delay of basic logic gates comprising of such non-classical nano-CMOS transistors.

High-K Dielectrics in CMOS Technology

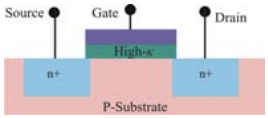
- Several materials have been investigated for use in nano-CMOS technology, such as ZrO2, TiO2, BST, HfO2, Al2O3, SiON, and Si3N4.
- Intel has recently prototyped a processor called Penryn using such transistors of 45nm technology.
- For compact modeling based study of high-K non-classical transistors using BSIM4/5, two possible options can be considered:

(i) varying the model parameter in the model card that denotes relative permittivity (EPSROX)

(ii) finding the equivalent oxide thickness (EOT) for a dielectric under consideration.



Transistor with SiO2 gate dielectric



Transistor with High−K gate dielectric

Analysis of Logic Gates

- Calculated by evaluating both the source and drain components.
- For a MOS, Iox = (Igs +Igd +Igcs +Igcd +Igb).
- Values of individual components depends on states: ON, OFF, or transition

Four different states for 2-input NAND:

$$I_{ox,\,Logic}(State) = \sum_{MOS,i} I_{ox,\,i} \qquad I_{ox,\,Logic}\,(State)$$

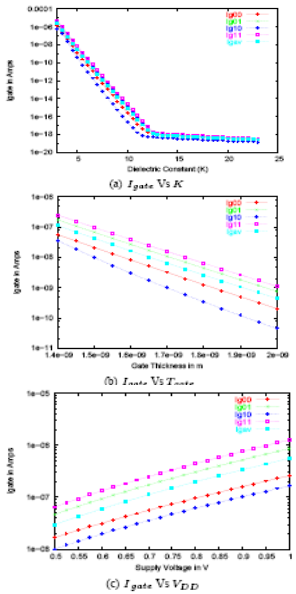
$$I_{00} \quad I_{01} \quad I_{10} \quad I_{11}$$

While characterizing the gate leakage current we present its average value over various switching states of the device.

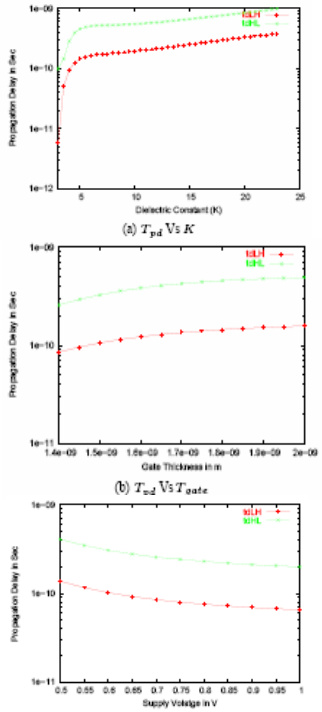
$$I_{tun} = \frac{1}{4}(I_{00} + I_{01} + I_{10} + I_{11})$$

The effect of varying dielectric material was modeled by calculating an equivalent oxide thickness (T*ox) according to the formula:

T*ox = (Kgate / Kox) Tgate



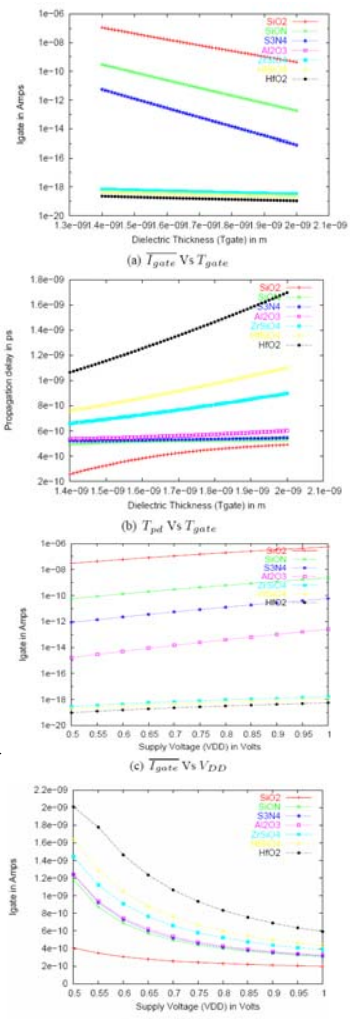
Gate leakage for a 2-input NAND logic gate for different states.



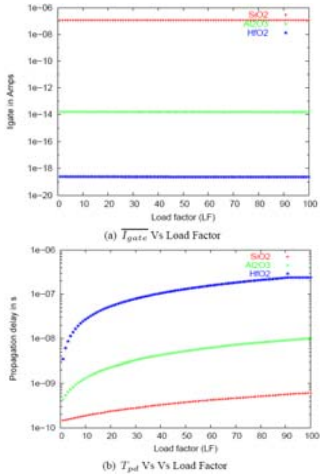
Low-to-high and high-to-low propagation delay for a 2-input NAND logic gate for different states.

Logic Gates with Specific High-K CMOS

- The effect of process variation on the gate tunneling current and propagation delay for various dielectric is studied.
- Among the dielectrics considered, HfO2 has the highest dielectric constant (K=22) while SiO2 has the lowest (K=3.9).
- Supply voltages varied from0.5V to 1.0V.
- Tgate varied from 1.4nm to 2.0nm.
- Loading condition also varied for analysis.



Evaluation of selected gate dielectrics



Effect of capacitive load

Logic Level Analytical Modeling

- We performed curve-fitting of the data for each attribute viz. K, Tgate, and VDD for their effect on gate tunneling current and propagation delay.
- The results of this modeling can be used in back-end tools of design and automatic synthesis frameworks for on-the-fly calculation.

Table 1. Curve Fitting for effect of Process and Design Variation in 2-input NAND

Attributes	Fitting Functions	Function Parameters
$\overline{T_{gate}}$ Vs K	$\overline{T_{gate}} = A * exp\left(\frac{-K}{\alpha}\right) + \overline{T_{gate_0}}$	$\overline{T_{gate_0}} = -4.6 * 10^{-9}$ $A = 0.00966, \alpha = 0.36115$
T_{pd} Vs K	$T_{pd} = \begin{cases} A_2 + \frac{A_1 - A_2}{1+exp\left(\frac{K-K_0}{\alpha}\right)}, & 2.5 \le K < 6 \\ A_3 * exp\left(\frac{-K}{\alpha}\right) + T_{pd_0}, & 6 \le K < 30 \end{cases}$	$A_1 = 4.12 * 10^{-11}, A_2 = 5.14 * 10^{-10}$ $K_0 = 4.02176, \alpha = 0.47847$ $A_3 = 6.94 * 10^{-11}, \beta = -10.63$ $T_{pd_0} = 3.75 * 10^{-10}$
$\overline{T_{gate}}$ Vs T_{gate}	$\overline{T_{gate}} = A * exp\left(\frac{-K}{\alpha}\right) + \overline{T_{gate_0}}$	$\overline{T_{gate_0}} = 3.13 * 10^{-10}$ $A = 0.09475, \alpha = 1.03 * 10^{-10}$
T_{pd} Vs T_{gate}	$T_{pd} = \frac{A+B*T_{gate}{}^{1-\alpha}}{1+B*T_{gate}{}^{1-\alpha}}$	$A = 5.10110^{35}, B = 1.50110^{75}$ $\alpha = -7.49133$
$\overline{T_{gate}}$ Vs V_{DD}	$\overline{T_{gate}} = A * exp\left(\frac{V_{DD}}{\alpha}\right) + \overline{T_{gate_0}}$	$\overline{T_{gate_0}} = -2.47 * 10^{-08}$ $A = 4.76 * 10^{-9}, \alpha = 0.20795$
T_{pd} Vs T_{gate}	$T_{pd} = A * exp\left(\frac{-T_{gate}}{\alpha}\right) + T_{pd_0}$	$T_{pd_0} = 1.92 * 10^{-10}$ $A = 4.21 * 10^{-9}, \beta = 0.16781$

Conclusions

- We presented a comprehensive analysis of the transient behavior of a CMOS logic gates for a 45nm BSIM4 model.
- A first principle physics based approach will be used followed by TCAD based simulations for validation.