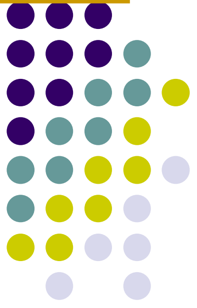

Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates

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Dept of Computer Science and Engineering
University of North Texas, Denton, TX, 76203.
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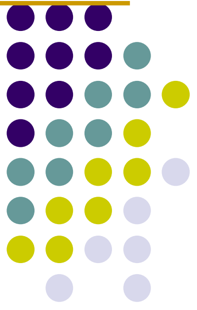
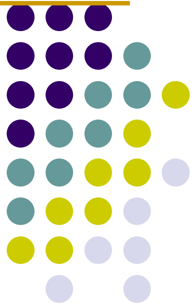
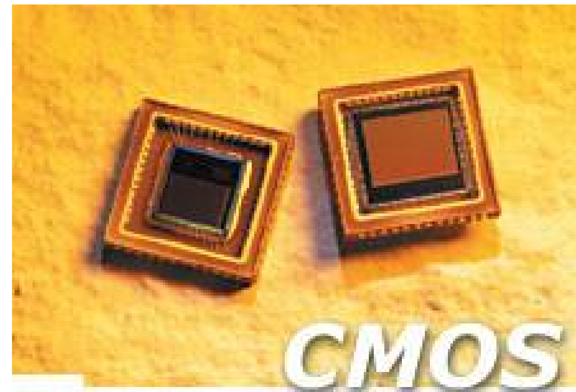
Outline of the Talk

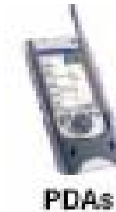


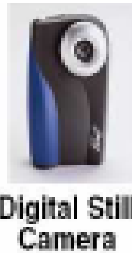
- CMOS scaling –Trends and Effects
- Power consumption redistribution due to scaling
  - Components of Power Dissipation
  - Components of Leakage
- Gate leakage analysis – Proposed Metrics
- Gate leakage variation with process and design parameters

CMOS Driven Applications

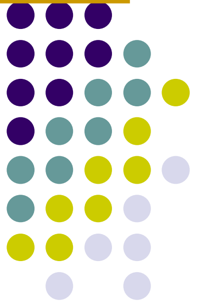






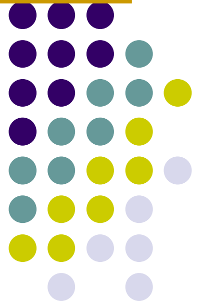


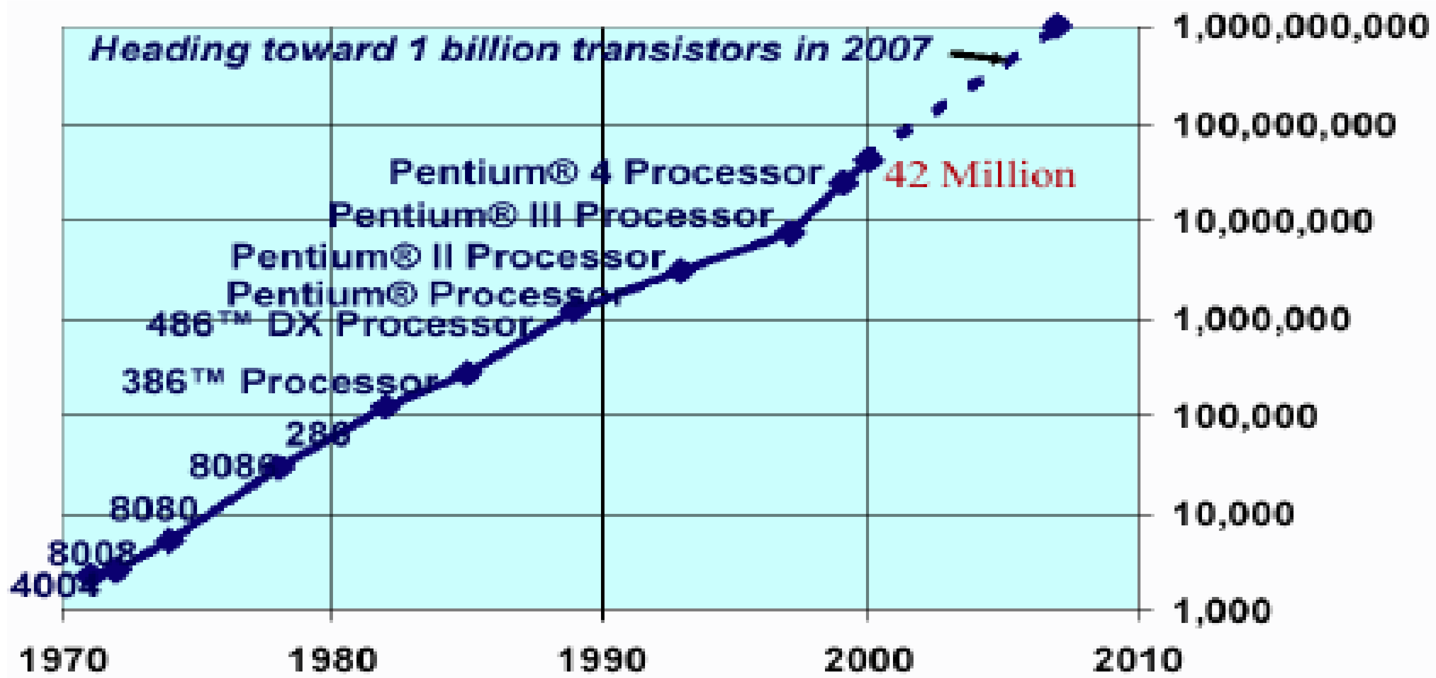
Almost the entire industrial revolution today is driven by CMOS.



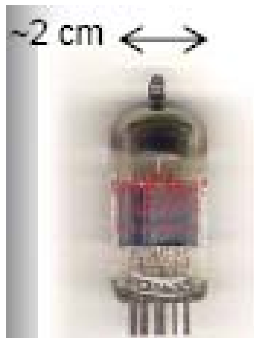
CMOS Technology Scaling and Power Dissipation Redistribution

Scaling Trend – Transistor Count

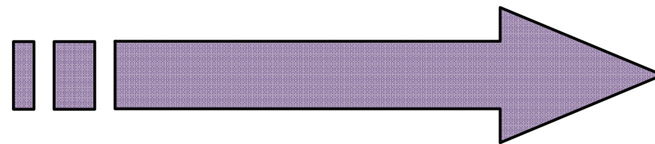




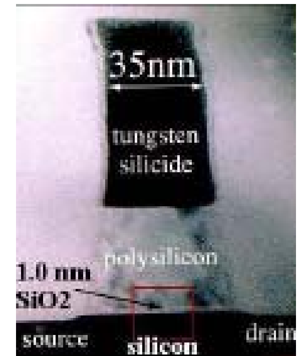
Increase in Transistor Count per chip



1967

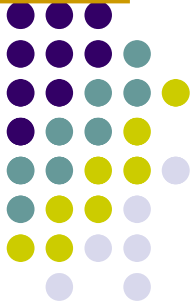


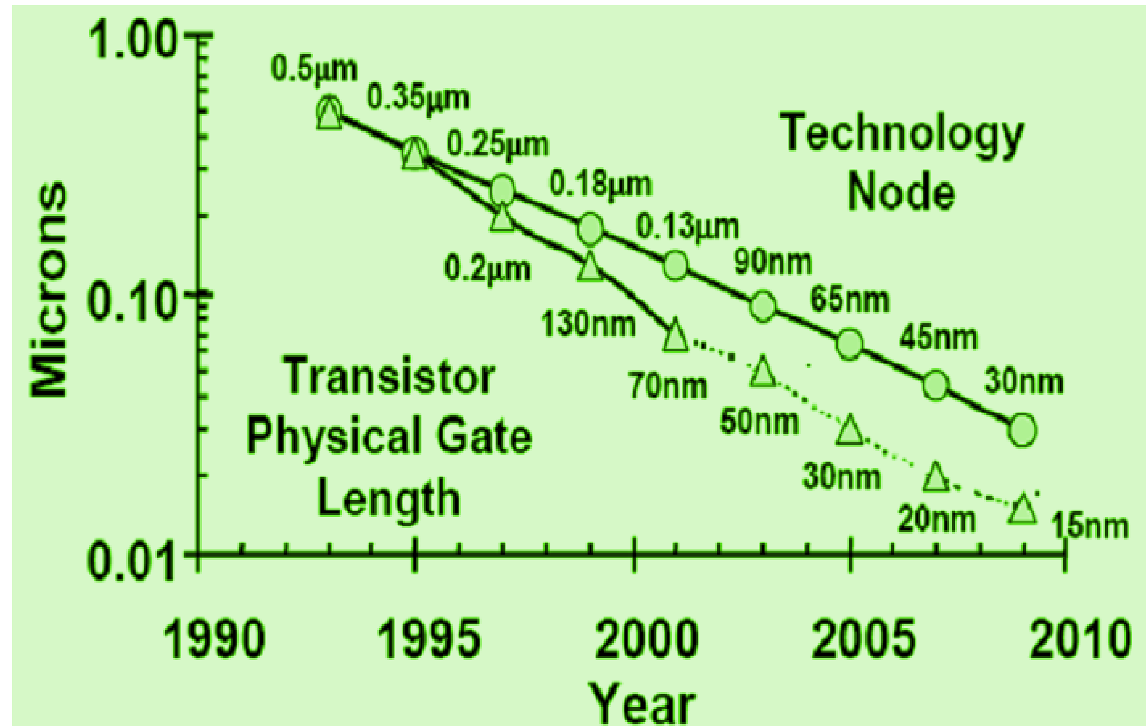
VLSI technology is the fastest growing technology in the human history.



2007

What is Physically Scaled ? (Gate Length)

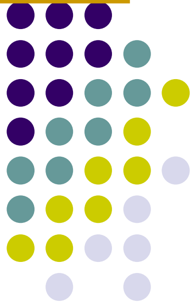




- Gate length of the transistor has been decreasing with technology scaling.
- All the other dimensions including gate oxide thickness have been scaled down to support this trend.

Source: Pedram ASPDAC 2004, Osburn IBM JRD Mar2002

Other Parameters Scaled?



Supply and Threshold Voltages (V)

10, 5, 2, 1, 0.5, 0.2, 0.1

V_{dd}

V_{th}

T_{ox}

Supply Voltage

Threshold Voltage

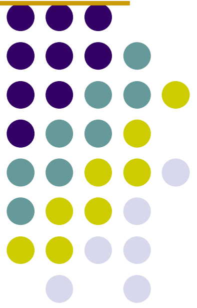
Gate Oxide Thickness

1, 0.5, 0.2, 0.1, 0.02

Channel Length (μm) →

Source: Taur IBM JRD MAR 2002

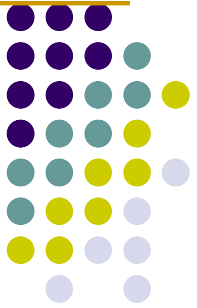
Power Dissipation Components in Nano-CMOS



- **Total Power Dissipation**
  - **Static Dissipation**
    - Sub-threshold current
    - Tunneling current
    - Reverse-biased diode Leakage
    - Contention current
  - **Dynamic Dissipation**
    - Capacitive Switching
    - Tunneling current
    - Short circuit

Source: Weste and Harris 2005

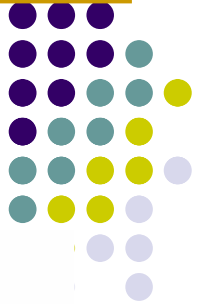
Leakages in Nanoscale CMOS



- I_1 : reverse bias pn junction (both ON & OFF)
- I_2 : subthreshold leakage (OFF)
- I_3 :oxide tunneling current (both ON & OFF)
- I_4 : gate current due to hot carrier injection (both ON & OFF)
- I_5 : gate induced drain leakage (OFF)
- I_6 : channel punch through current (OFF)

Source: Roy Proceedings of IEEE Feb2003

Power Dissipation: Redistribution



Gate Length

Normalized Power Dissipation

10^{2}
10^{0}
10^{-2}
10^{-4}
10^{-6}

Sub-Threshold

Tunneling

Dynamic

Gate leakage will predominate for sub 65-nm technology.

300
250
200
150
100
50
0

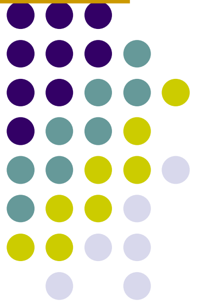
Physical Gate Length (nm)

1990 1995 2000 2005 2010 2015 2020

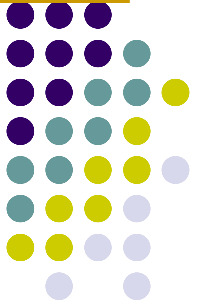
Chronological (Year) →

Source: Hansen 2004

Scaling Trends and Effects: Summary

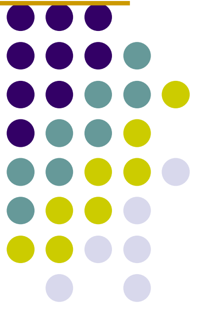


- Scaling improves
  - Transistor Density of chip
  - Functionality on a chip
  - Speed, Frequency, and Performance
- Scaling and power dissipation
  - Active power remains almost constant
  - Components of leakage power increase in number and in magnitude.
  - Gate leakage (tunneling) predominates for sub 65-nm technology.



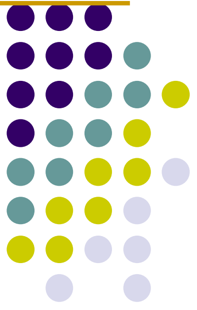
Contributions of Our Paper
and
Related Research

Contributions of Our Paper



1. Both ON and OFF state gate leakage are significant.
2. During transition of states there is transient effect is gate tunneling current.
3. New metrics: I_{tun} and C_{tun}
4. C_{tun}: Manifests to intra-device loading effect of the tunneling current
5. NOR Vs NAND in terms of I_{tun} and C_{tun}
6. Study process/design variation on I_{tun} and C_{tun}

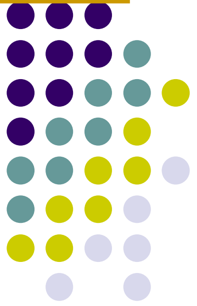
Contributions of Our Paper (Salient Feature)



A new metric, the effective tunneling capacitance essentially quantifies the intra-device loading effect of the tunneling current and also gives a qualitative idea of the driving capacity of the logic gate.

How to quantify it at transistor and logic-gate level??

Gate Capacitance of a Transistor (Intrinsic)

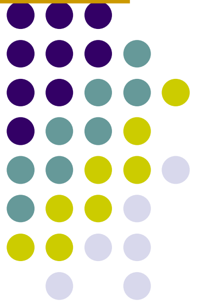


G

C_{gs} C_{gb} C_{gd}

S B D

Gate Capacitance of a Transistor (Tunneling: Proposed)



G

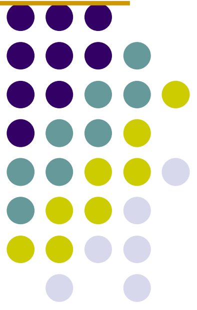
C_{gs}^{tun} C_{gb}^{tun} C_{gd}^{tun}

S D

C_{gcs}^{tun} B C_{gcd}^{tun}

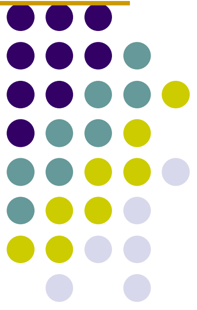
We propose that transient in gate tunneling current due to state transitions are manifested as capacitances.

Related Research Works (Gate Leakage Analysis)



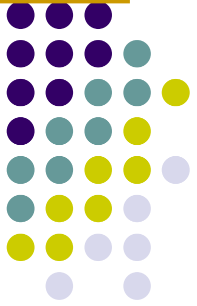
- Ghibaudo 2004: Characterization and modeling issues of ultra thin oxide devices
- Mukhopadhyay 2003: Characterization methodology is proposed along with reduction
- Yang 1999: Direct tunneling current and CV measurements in MOS devices used to model
- Hertani 2005: Provide leakage analysis of NAND, NOR, XOR gates

Related Research Works



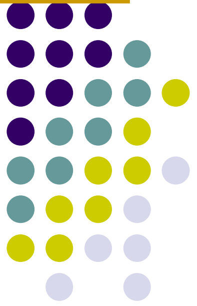
- No work characterize both ON and OFF
- No work examine the device or a logic gate when it changes stated:

ON→OFF or OFF→ ON



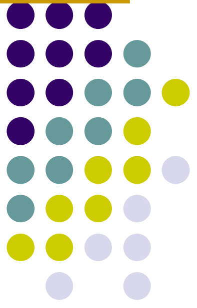
Analysis
in
a
CMOS Transistor

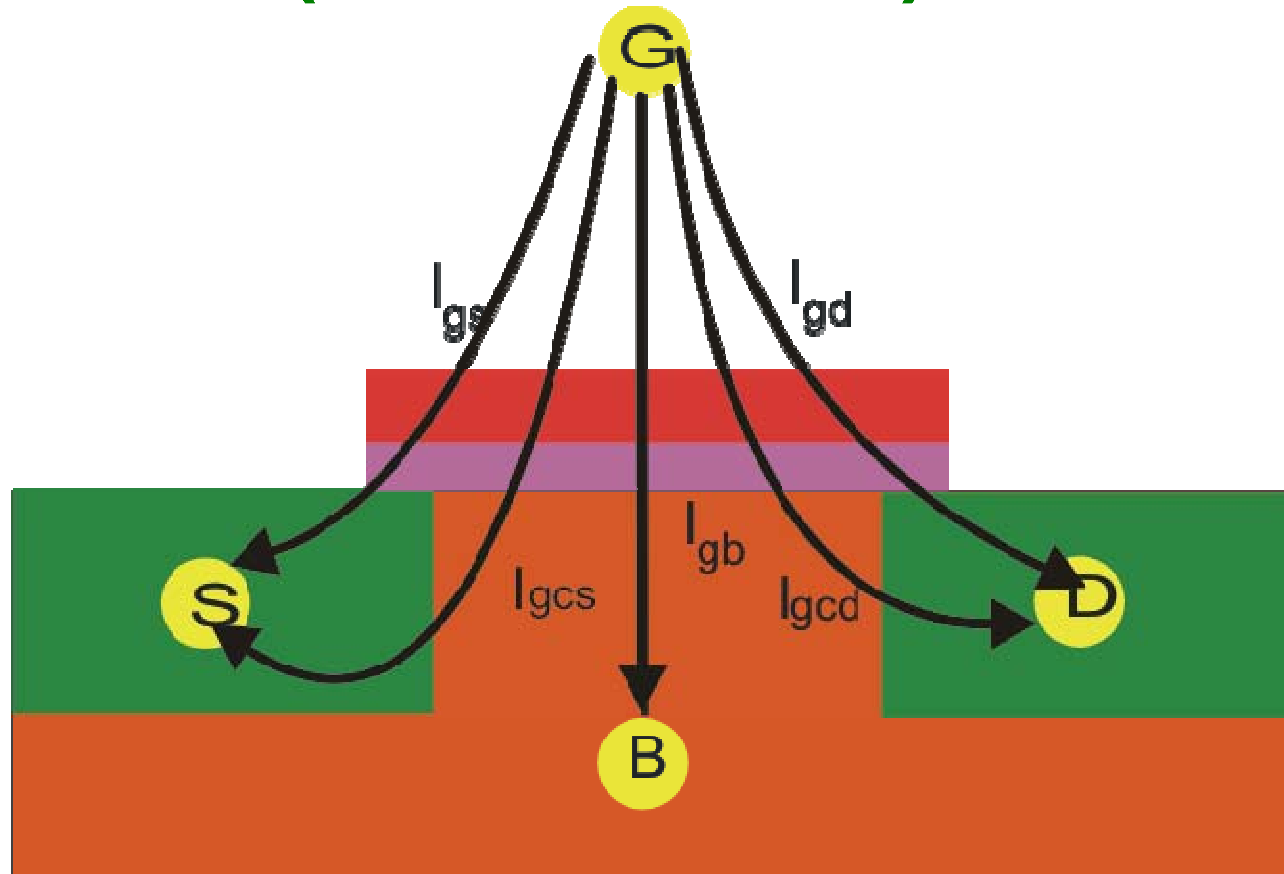
Outline: Transistor Level



- Dynamics of gate oxide tunneling in a transistor
- SPICE model for gate leakage
- ON, OFF, and transition states of a transistor
- Gate leakage in ON, OFF, and transition states of a transistor

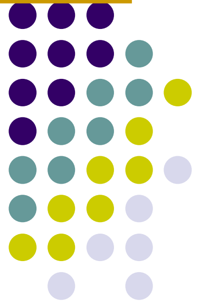
Gate Leakage Components (BSIM4 Model)





- I_{gs}, I_{gd}: tunneling through overlap of gate and diffusions
- I_{gcs}, I_{gcd}: tunneling from the gate to the diffusions via channel
- I_{gb}: tunneling from the gate to the bulk via the channel

NMOS Transistor: ON



G

I_{gs}

V_{dd}

S

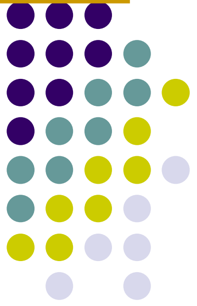
I_{gcs}

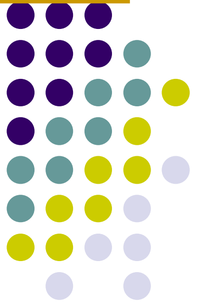
I_{gcd}

D

B

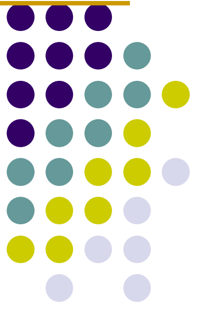
NMOS Transistor: OFF





NMOS Transistor: Transition

Gate Leakage for a MOS: I_{ox}



- Calculated by evaluating both the source and drain components
- For a MOS, $I_{ox} = (|I_{gs}| + |I_{gd}| + |I_{gcs}| + |I_{gcd}| + |I_{gb}|)$
- Values of individual components depends on states: ON, OFF, or transition

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NMOS Gate Leakage (For a Switching Cycle)

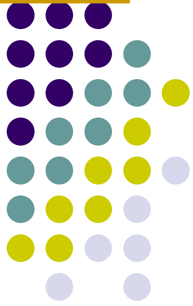


Fig. 1

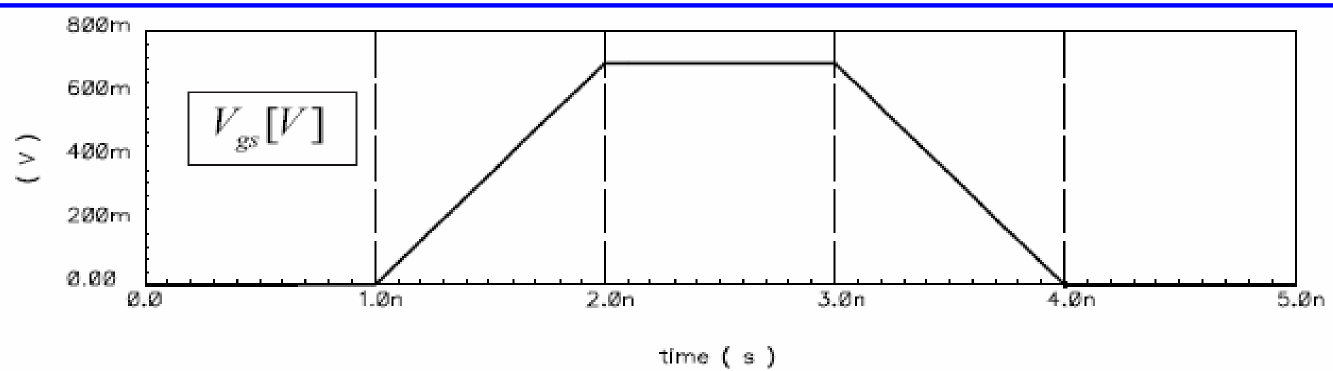


Fig. 2

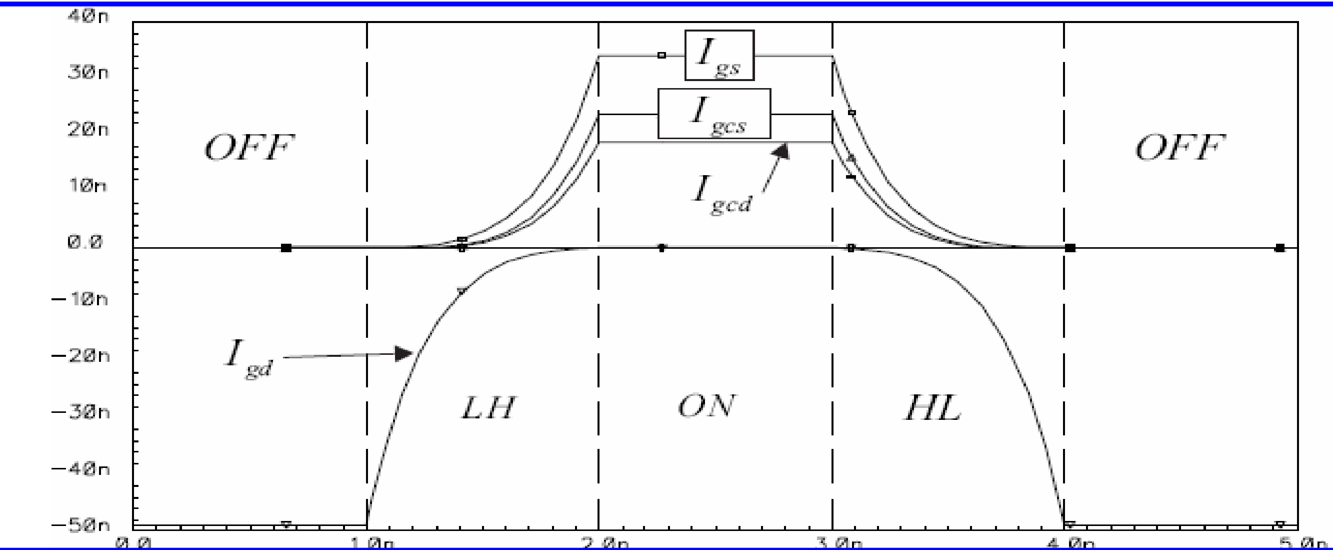
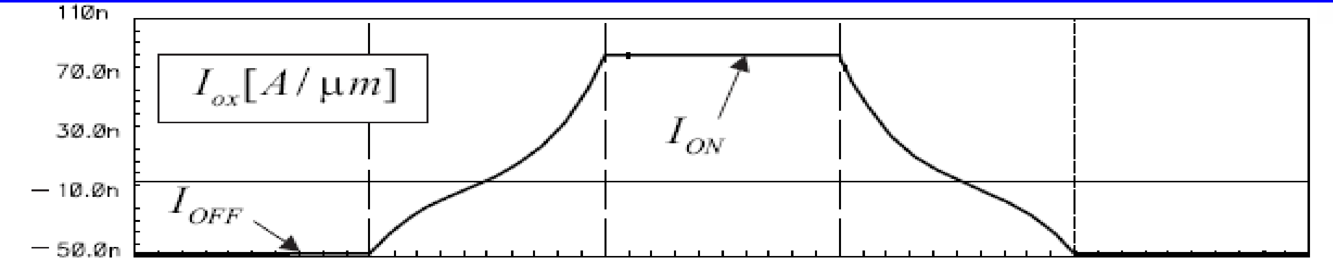
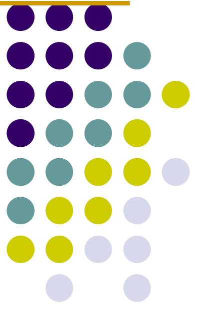


Fig. 3

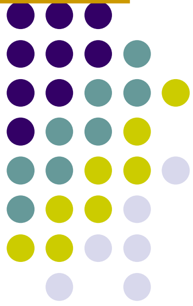


NMOS Gate Leakage (Observation and Metrics)

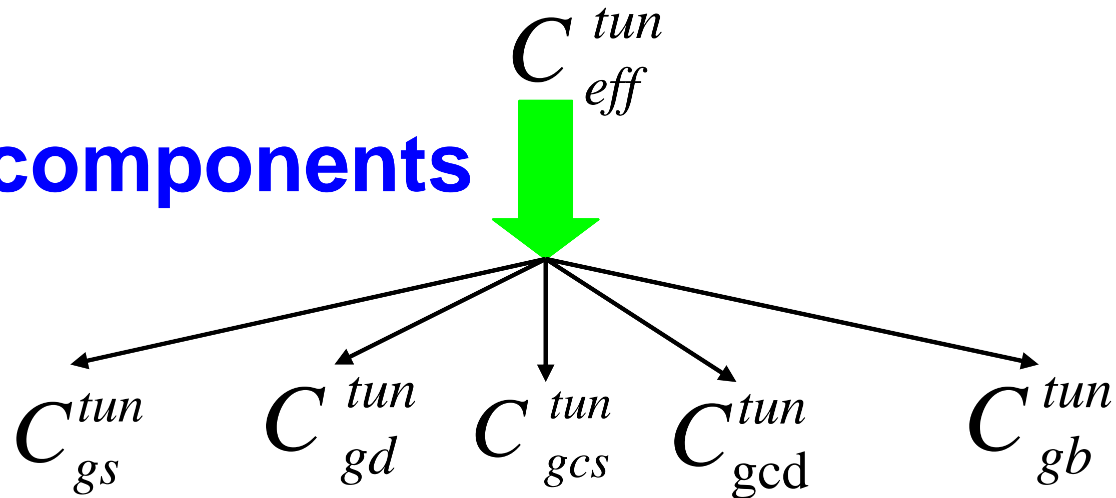


- Gate leakage happens in ON state: I_{ON}
- Gate leakage happens in OFF state: I_{OFF}
- Gate leakage happens during transition: C_{eff}^{tun}

NMOS Gate Leakage: C_{eff}^{tun}



5 components

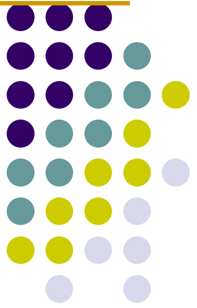


We propose to quantify as:

$$C_{eff}^{tun} = \frac{I_{ON} - I_{OFF}}{\left(\frac{dV_g}{dt}\right)}$$

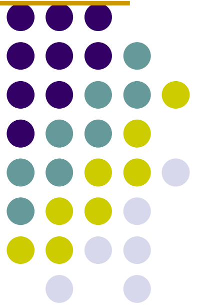
$$= \frac{I_{ON} - I_{OFF}}{V_{DD}} t_r \quad \text{(for equal rise/fall time)}$$

NMOS Gate Leakage: Summary

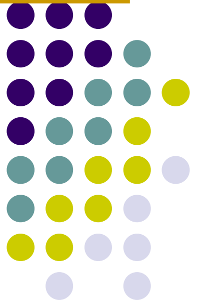


The behavior of the device in terms of gate tunneling leakage must be characterized not only during the steady states but also during transient states.

Transistor → Logic Gate

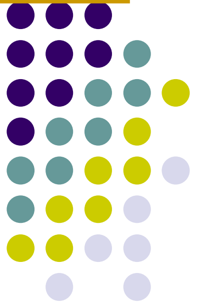


- How do we quantify the same metrics at logic level??
- State dependent or state independent??

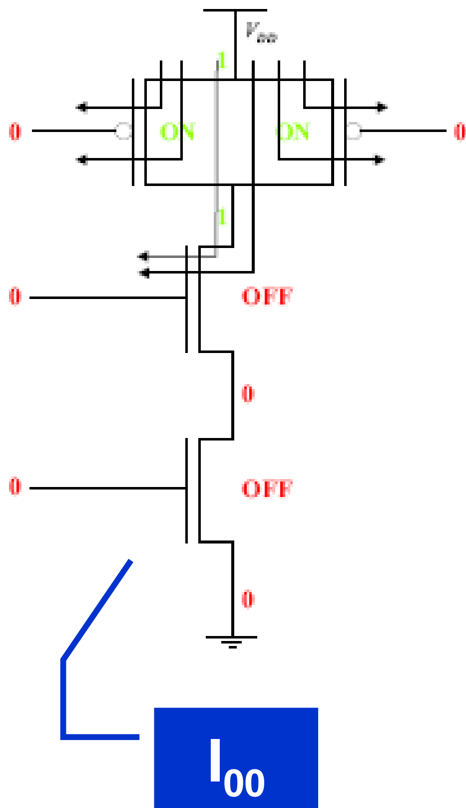


Analysis in Logic Gates

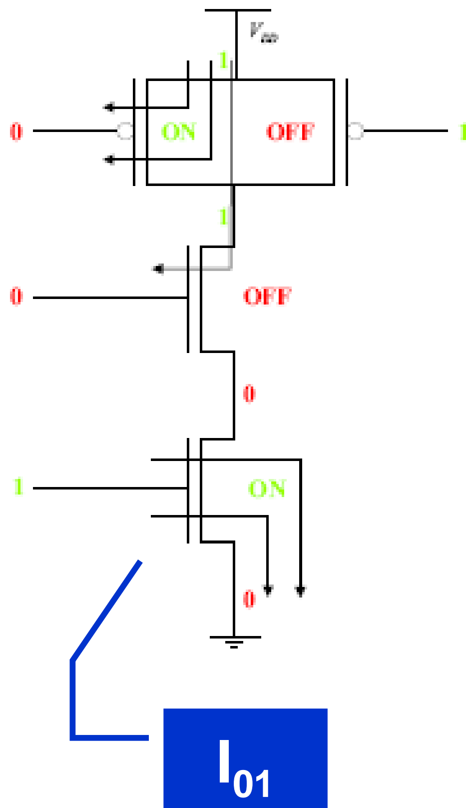
Gate Leakage in 2-input NAND (State Specific)



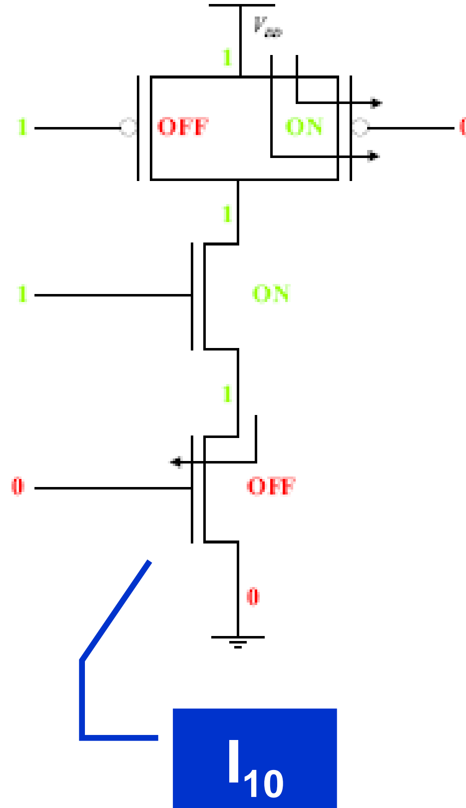
input 00



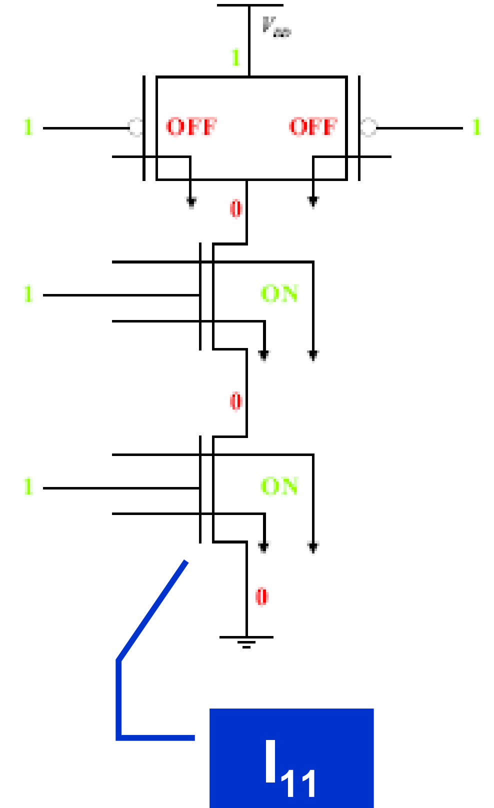
input 01



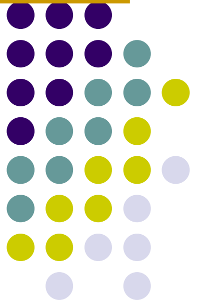
input 10



input 11

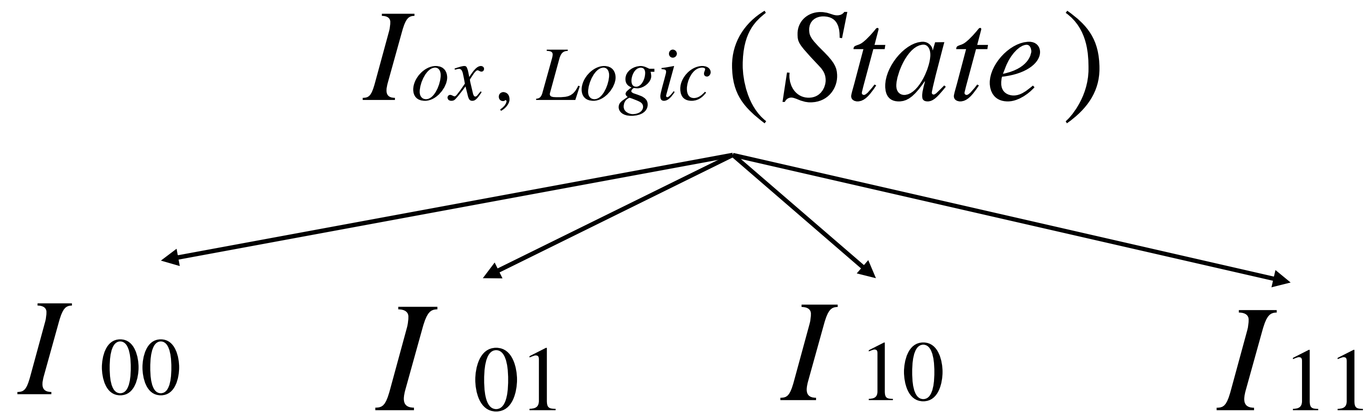


Gate Leakage in 2-input NAND (State Specific)

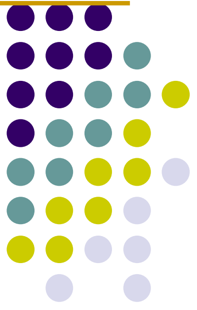


$$I_{ox,\,Logic}(State) = \sum_{MOS,\,i} I_{ox,\,i}$$

Four different states for 2-input NAND:



Gate Leakage in 2-input NAND (State Independent)

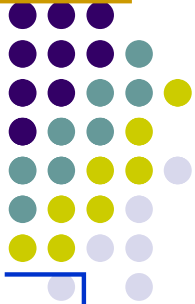


I_{tun} ≡ State Independent average gate leakage current of a logic gate

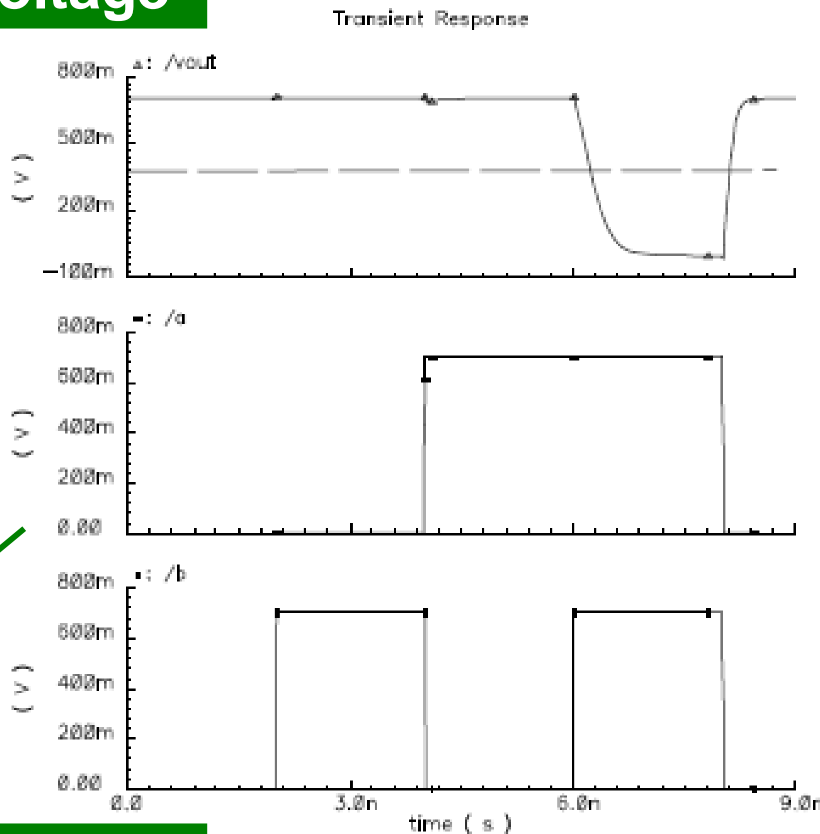
$$I_{tun} = \frac{1}{4}\left(I_{00} + I_{01} + I_{10} + I_{11}\right)$$

This is a measure of gate leakage of a logic gate during its steady state.

Gate Leakage in 2-input NAND (Transient Study)



Output Voltage

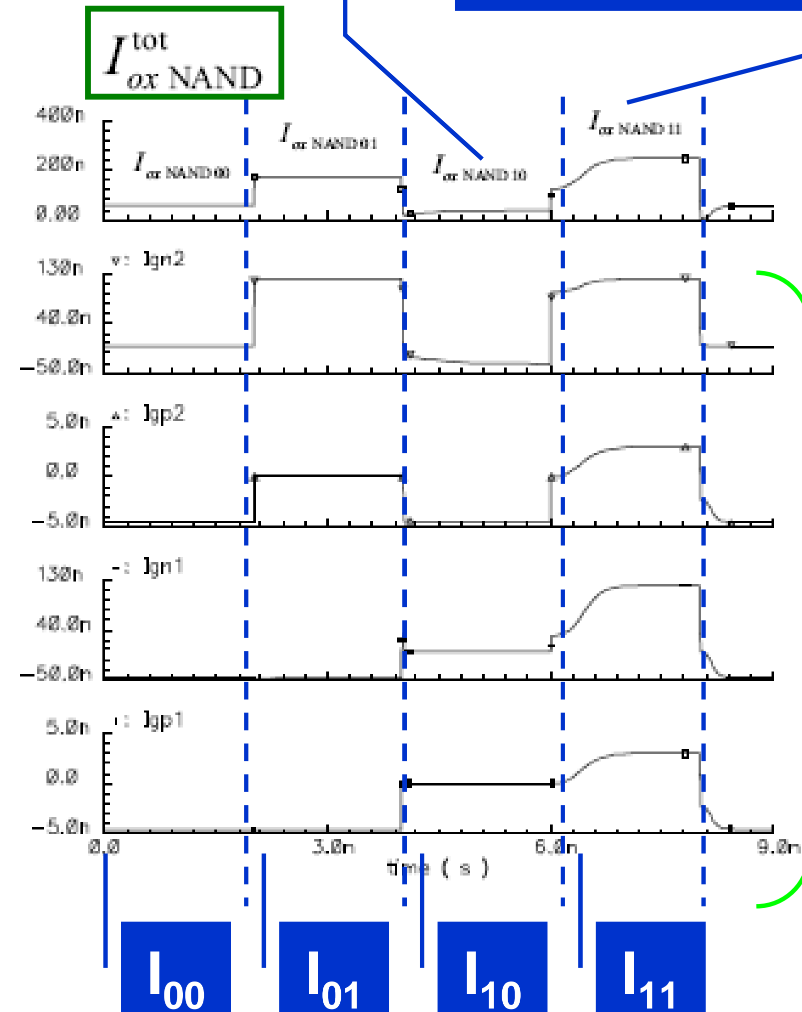


Input Voltages

Best Case

Worst Case

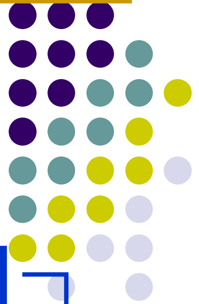
$I^{tot}_{ox\ NAND}$



I_{00} I_{01} I_{10} I_{11}

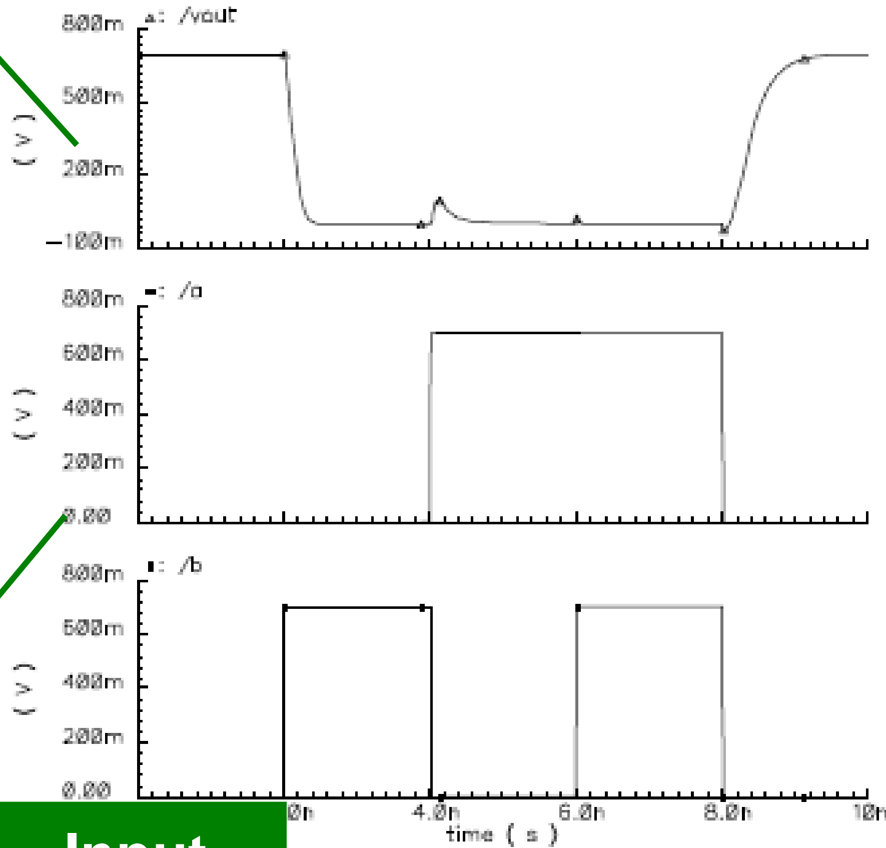
Gate Current in individual MOS

Gate Leakage in 2-input NOR (Transient Study)



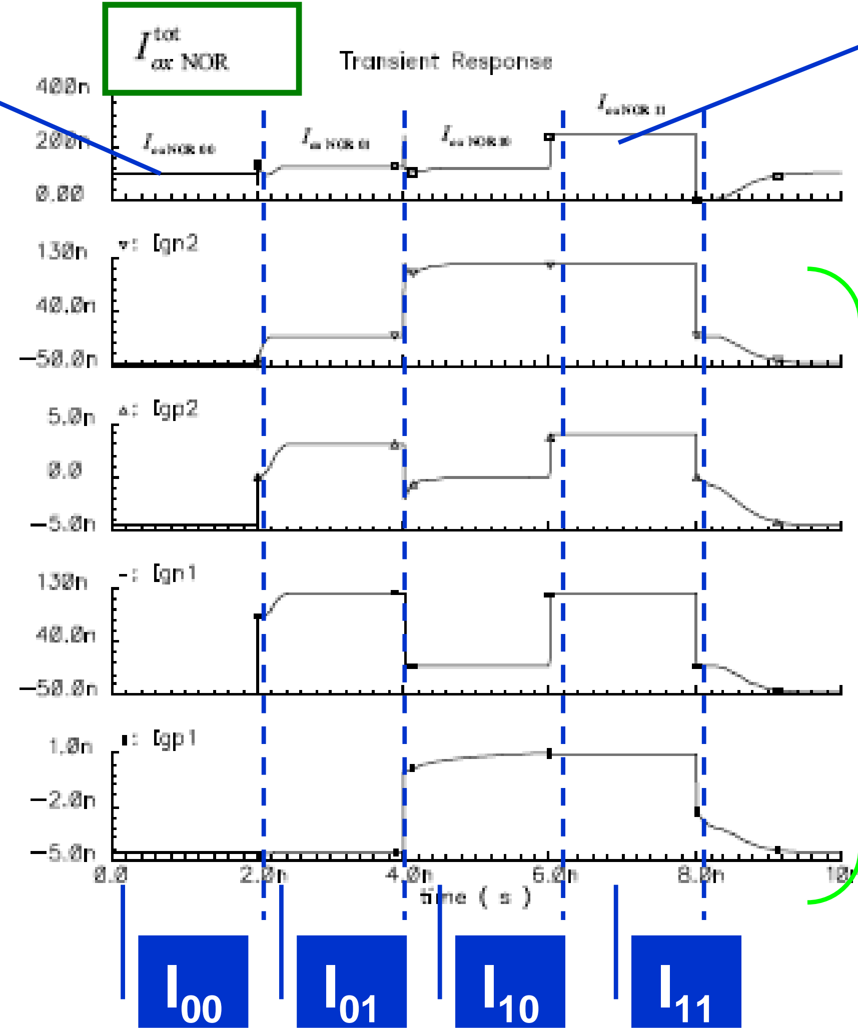
Output Voltage

Input Voltages



Best Case

Worst Case

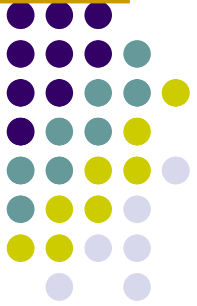


$I_{ox\,NOR}^{tot}$

Gate Current in individual MOS

I_{00} I_{01} I_{10} I_{11}

Gate Leakage in Logic Gate (Transient Study)

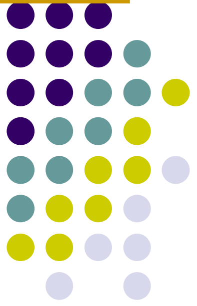


C_{tun} ≡ Effective tunneling capacitance at the input of a logic gate

We propose to quantify as:

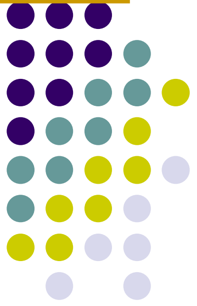
$$C^{tun} = \frac{I_{\max}^{\log ic} - I_{\min}^{\log ic}}{\left(\frac{dV_{in}}{dt}\right)}$$

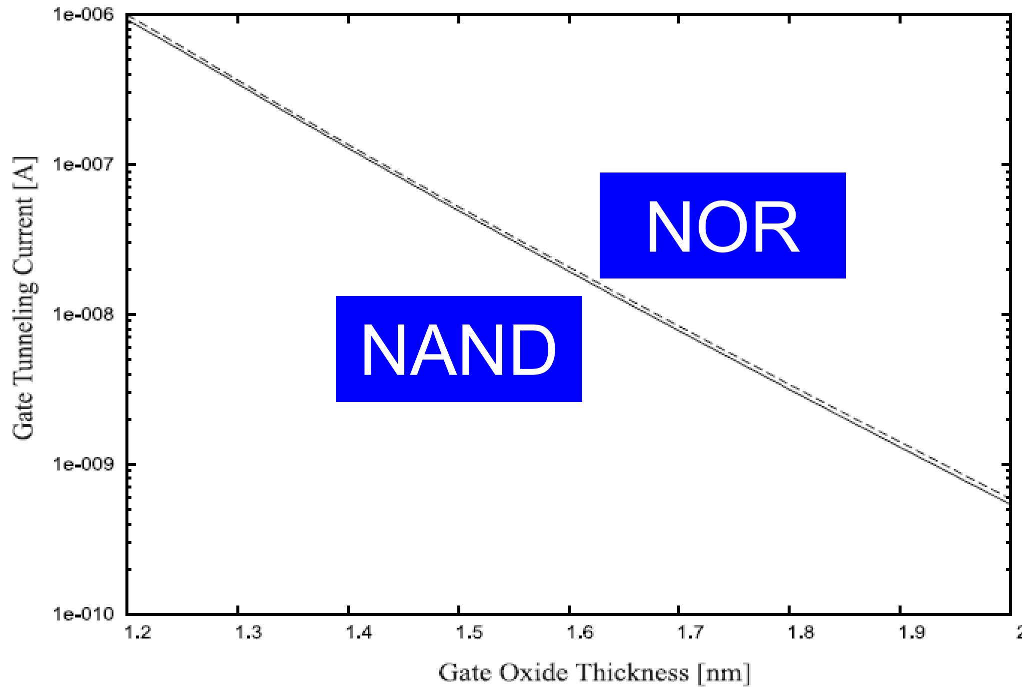
$$= \frac{I_{\max}^{\log ic} - I_{\min}^{\log ic}}{V_{DD}} t_r$$ (for equal rise/fall time)



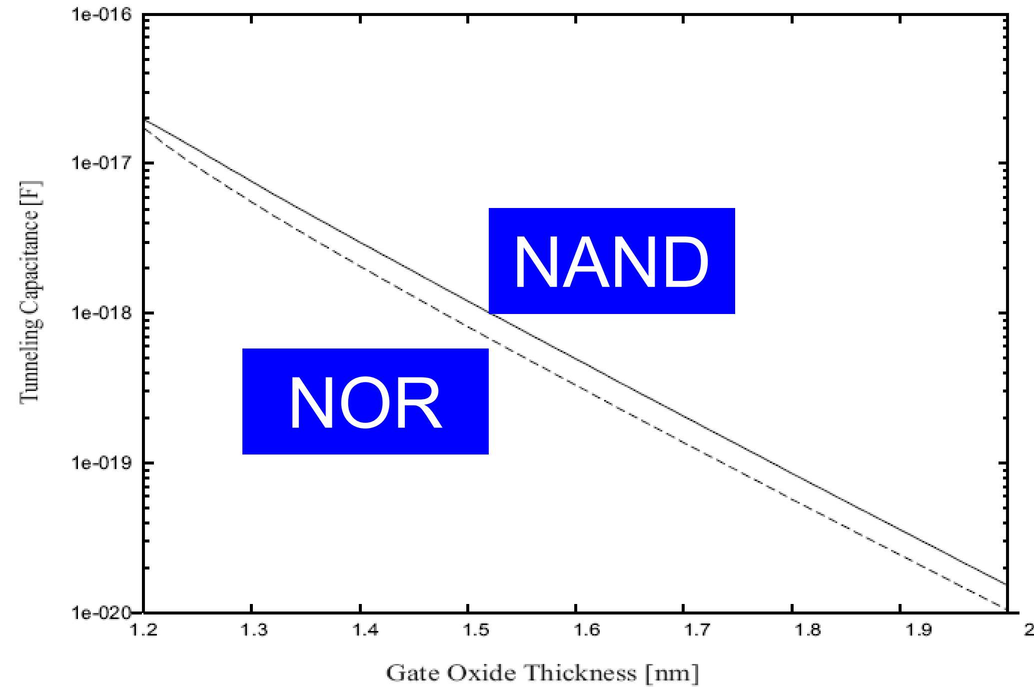
Effect of Process and Design Parameter Variation

Gate Leakage in 2-input Logic Gates (T_{ox} Variation)



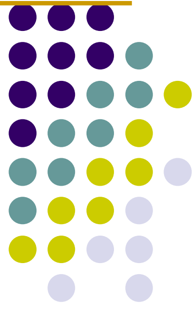


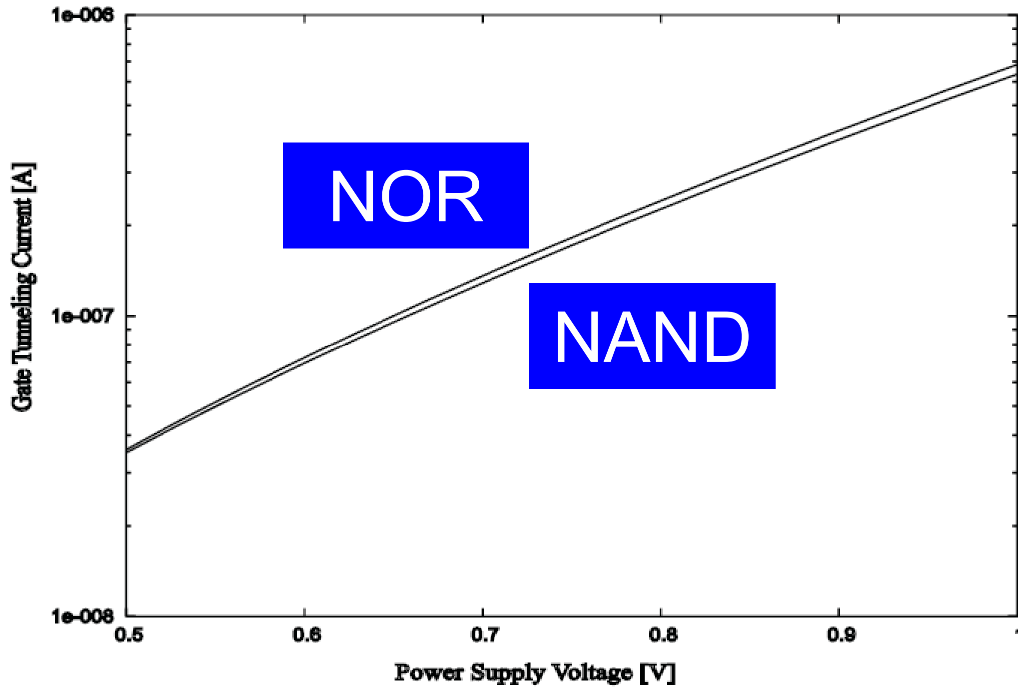
I_{tun} (logscale) versus T_{ox}



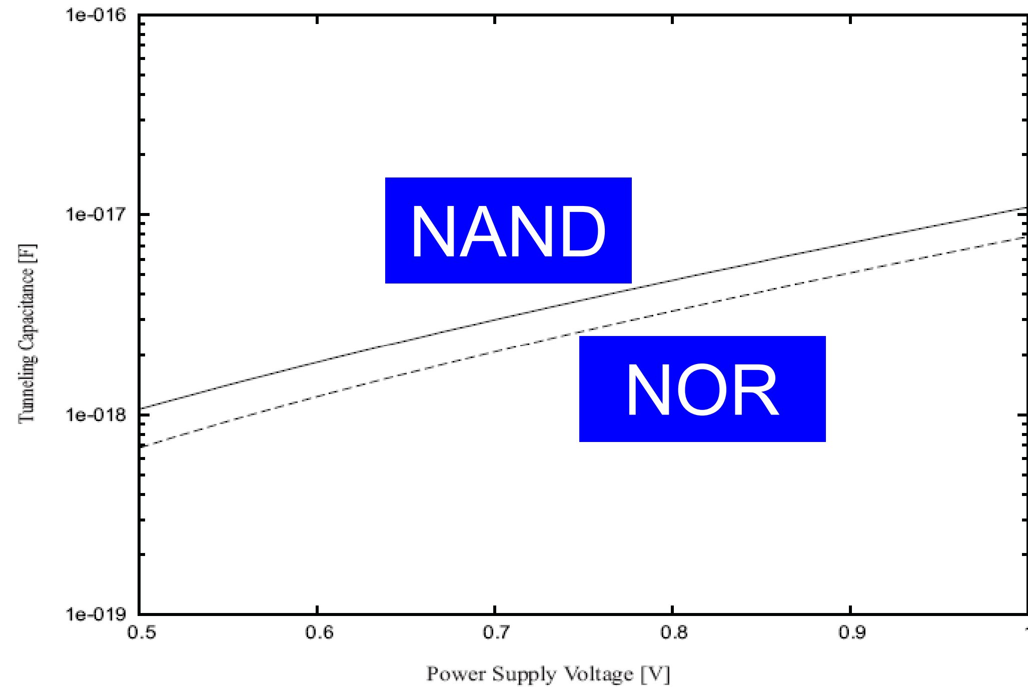
C_{tun} (logscale) versus T_{ox}

Gate Leakage in 2-input Logic Gates (V_{DD} Variation)

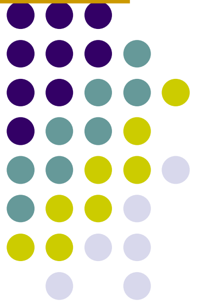




I_{tun} (logscale) versus V_{DD}

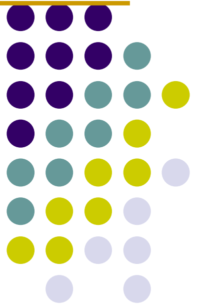


C_{tun} (logscale) versus V_{DD}



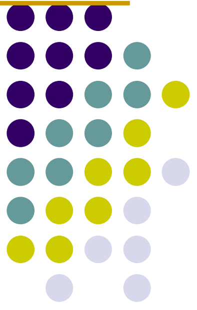
Summary and Conclusions

Gate Leakage in 2-input Logic Gates (Observation)



- Both ON and OFF states contribute to gate leakage
- Transient effect is significant and can be captured via effective tunneling capacitance
- I_{tun} ≡ State Independent average gate leakage current of a logic gate
- C_{tun} ≡ Effective tunneling capacitance at the input of a logic gate
- I_{tun} is larger for NOR
- C_{tun} is larger for NAND

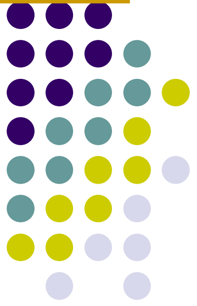
Usefulness of the Proposed Metrics



- The metrics allow designers to account for gate tunneling effect in nano-CMOS based circuit designs.
- I_{tun} - additive to static power consumption
- C_{tun} – additive to intrinsic gate capacitance

$$C_{logic} = C_{tun} + C_{intrinsic}$$

- All three needs to be taken into account for effective total (switching, subthreshold, gate leakage) power optimization



Thank You

For more information:

http://www.cse.unt.edu/~smohanty