# VLSI Design and CAD Research at University of North Texas

## Associated Laboratory

## VLSI Design and CAD Laboratory

**http://www.vdcl.cse.unt.edu**


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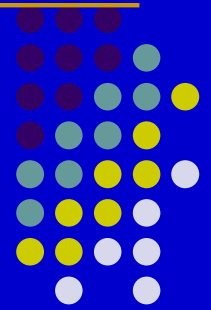
CSE

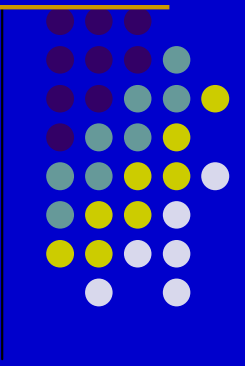
University of North Texas


# Outline of the Talk



- About VDCL
- Research Activity
- Publications
- Opportunities for Masters and Ph.D.


# VDCL



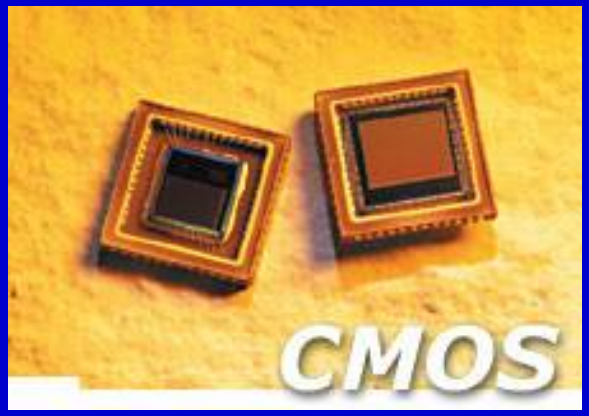
- Established in August 2004
- Mission:
  - to carry out research in low power VLSI design
  - to prepare next generation CAD tools for automatic design
- One Faculty, one associated Faculty, and six student members.
- Located at F233.
- State-of-art research infrastructure include Sun Fire server, Dual-Xeon Servers, Sun Workstations, Linux Workstations and Tera Bytes of storage.
- Licensed and free CAD tools available.

# CMOS Driven Applications

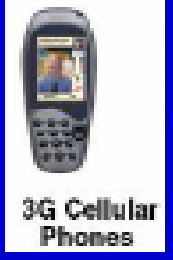














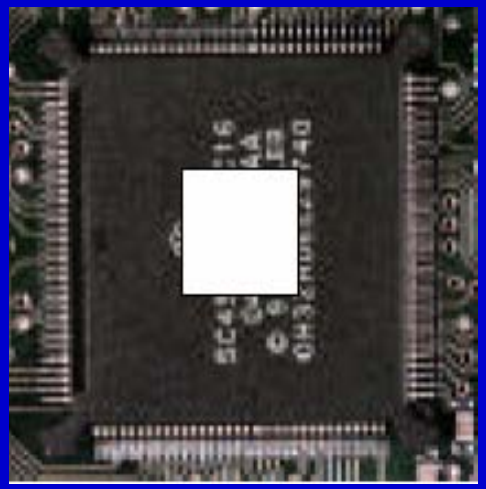


Almost the entire industry today is driven by CMOS

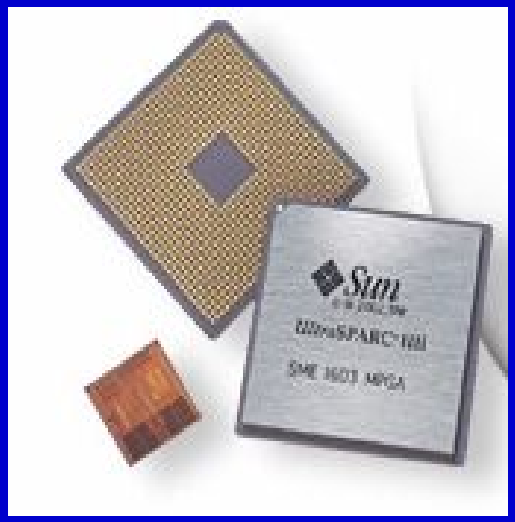
# What is an Integrated Circuit ?

- An integrated circuits is a silicon semiconductor crystal containing the electronic components for digital gates.
- Integrated Circuit is abbreviated as IC.
- The digital gates are interconnected to implement a Boolean function in a IC .
- The crystal is mounted in a ceramic/plastic material and external connections called “pins” are made available.
- ICs are informally called chips.

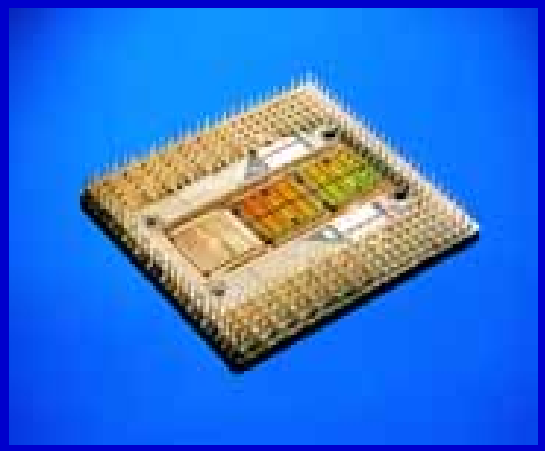
# How does a microprocessor look?



(1) ASIC

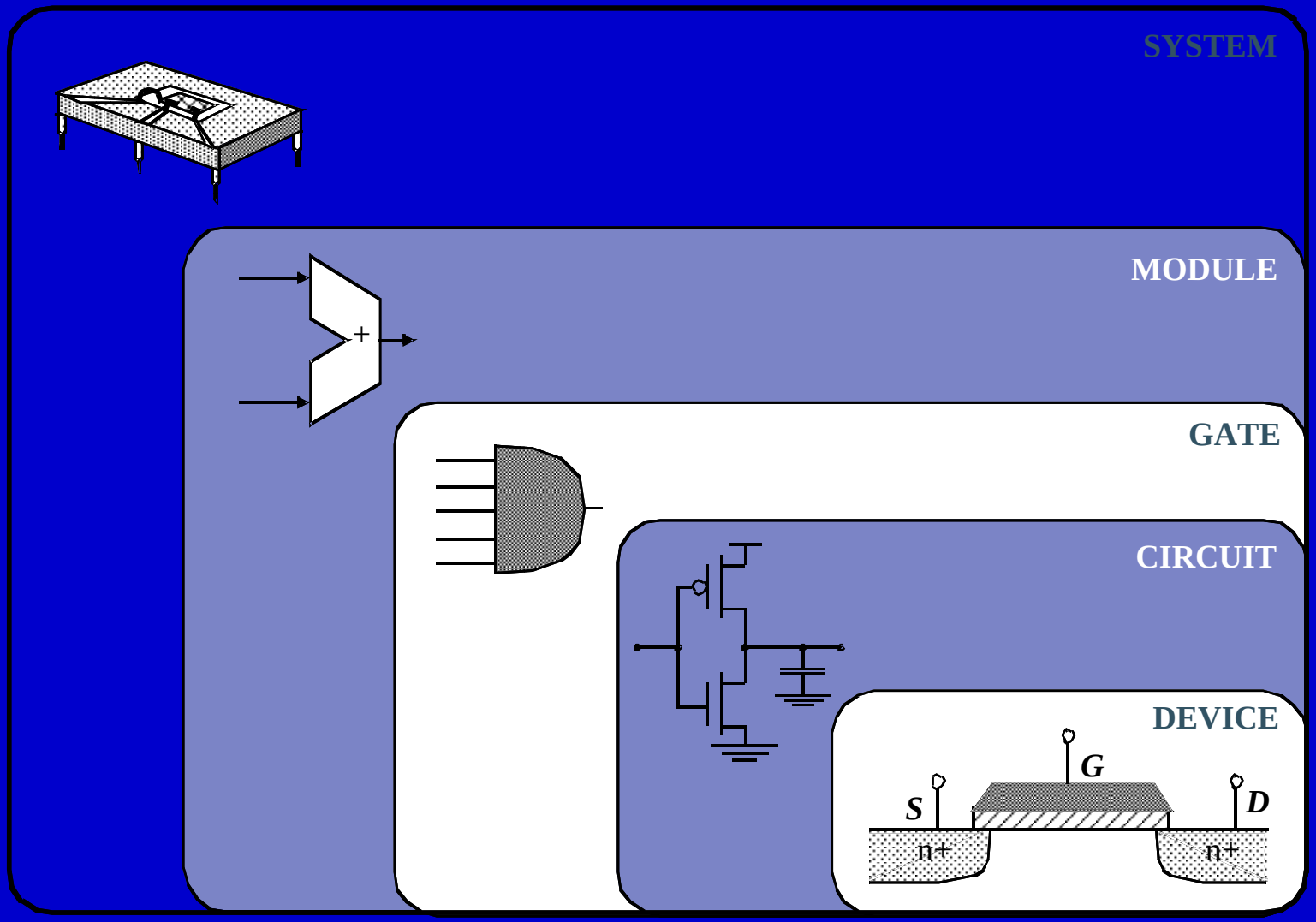



(2) Sun UltraSparc

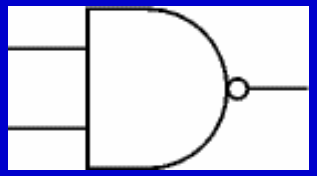


(3) PentiumPro

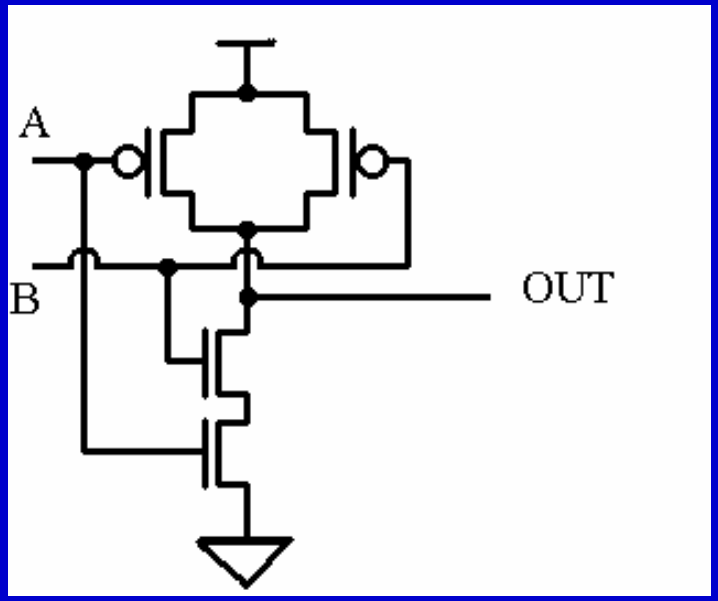
# Design Abstraction Levels



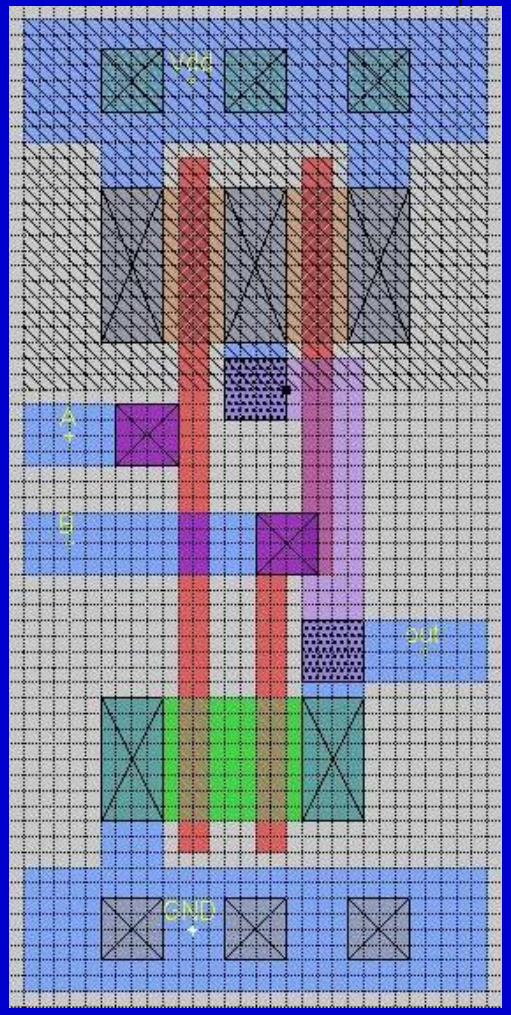
# Digital Circuits : Logic to Device



(NAND Gate)

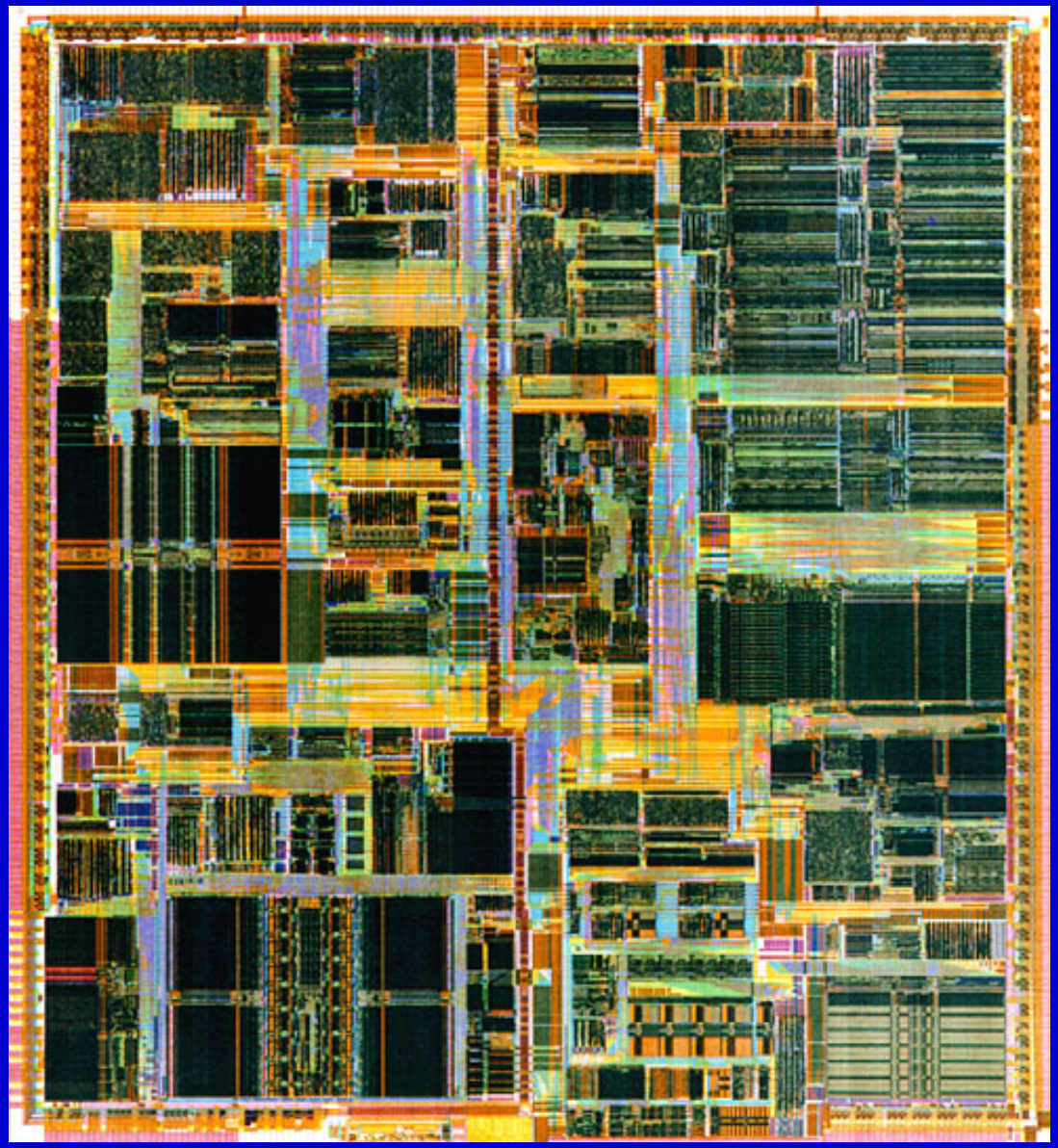



(Transistor Diagram)



(Layout Diagram)

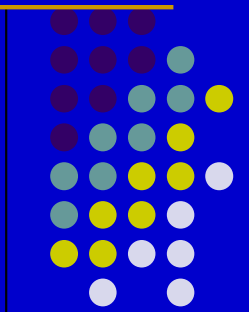
# Pentium IV : 52M Transistors (2001)



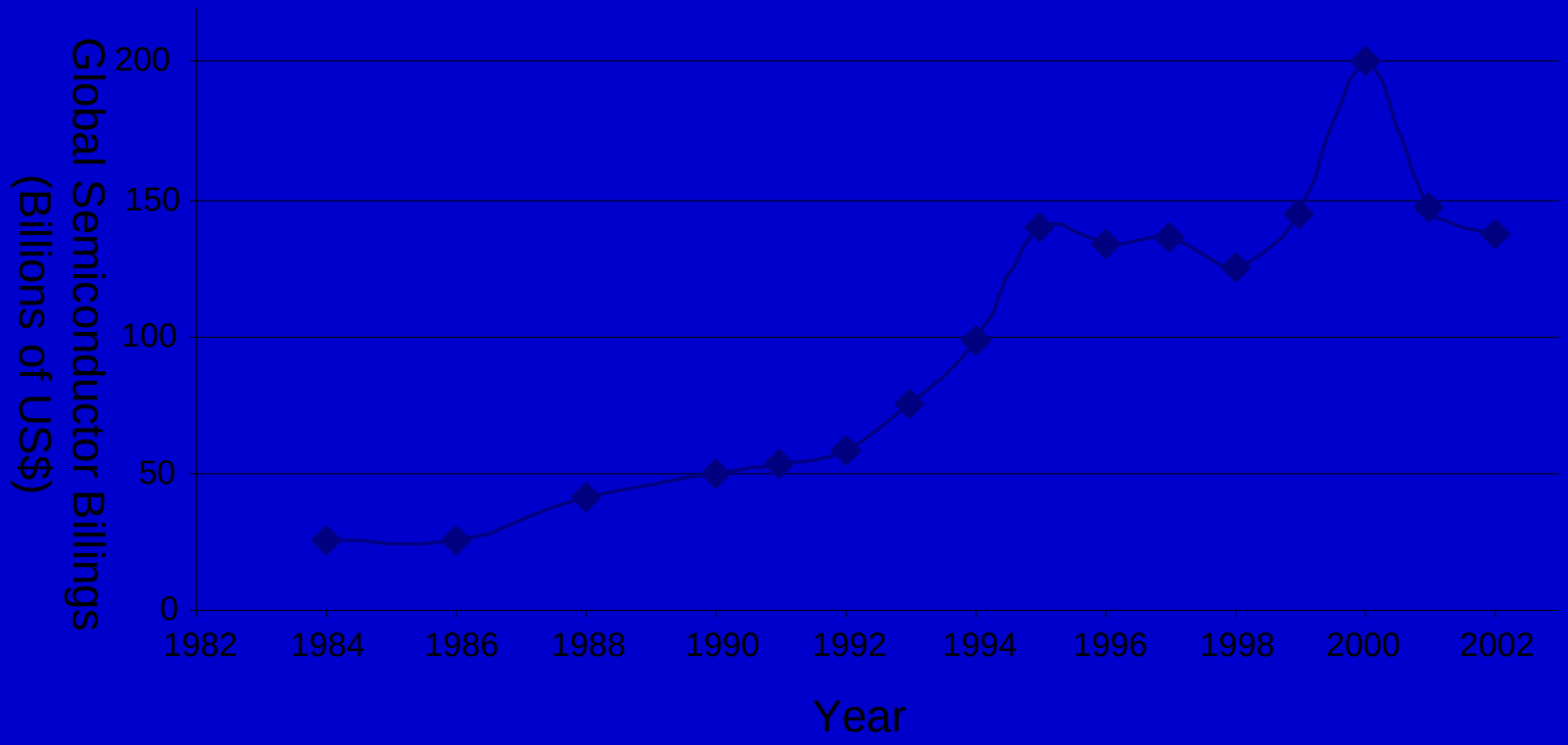
# VLSI Technology: Highest Growth in History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2003
  - Intel Pentium 4 μprocessor (55 million transistors)
  - 512 Mbit DRAM (> 0.5 billion transistors)
- 53% compound annual growth rate over 45 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power!
  - Revolutionary effects on society

# VLSI Industry : Annual Sales



- $10^{18}$ transistors manufactured in 2003
  - 100 million for every human on the planet




# Research Interests

- Synthesis and Optimization for Low Power
- Power Aware System Design
- VLSI Architecture for Security and Copyright Protection
- CAD and Modeling for Nanoscale VLSI Circuits

# Research Interests …

- Synthesis and Optimization for Low Power
  - Vary supply voltage, clock frequency, switching activity and capacitance, physical parameter through various phases of the synthesis process while considering their interactions and trade-offs.
- Power Aware System Design
  - Aim is to provide a low power, high performance architecture followed by its VLSI implementation for different applications, such as image and video processing, and wireless system

# Research Interests …

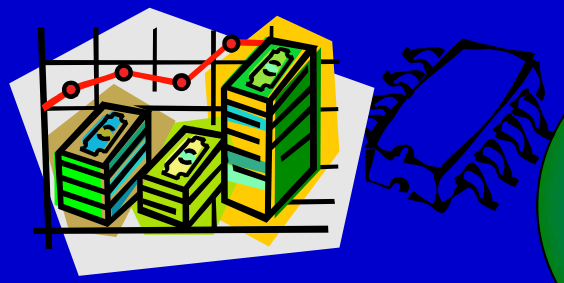
- VLSI Architecture for Security and Copyright Protection
  - Goal is to develop architectures to perform compression, encryption, watermarking and scrambling in a common hardware.
- CAD and Modeling for Nanoscale VLSI Circuits
  - Plan is to develop models for fast characterization of architectural and logic cells made of non-classical CMOS.

# Why Low Power?

## Major Motivation

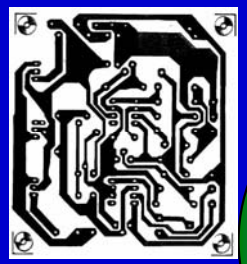
- Reducing Power Consumption
- Increasing Battery Life
- Making Portable Devices Really Portable…

# Why Low Power? …



Packaging costs

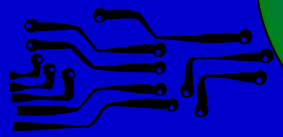
Chip and system cooling costs



Power supply rail design

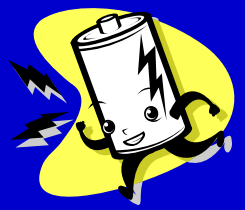
Power directly affects

Noise immunity and system reliability



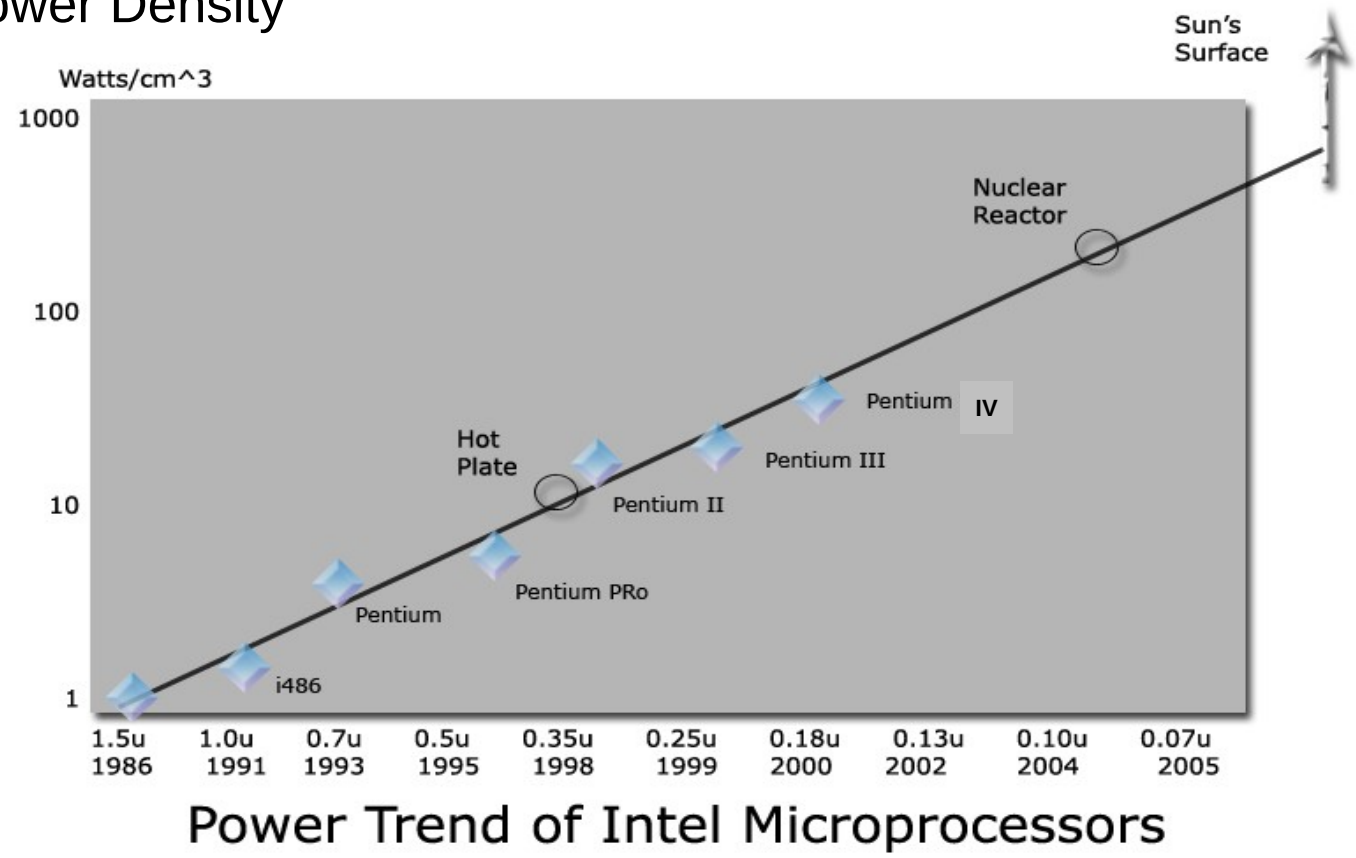
Environmental concerns

Battery life



# Why Low-Power ? …….

Power Density




Power Trend of Intel Microprocessors

# Power Dissipation Components in CMOS

**Total Power Dissipation**

**Static Dissipation**

- Sub-threshold current
- Tunneling current
- Reverse-biased diode Leakage
- Contention current

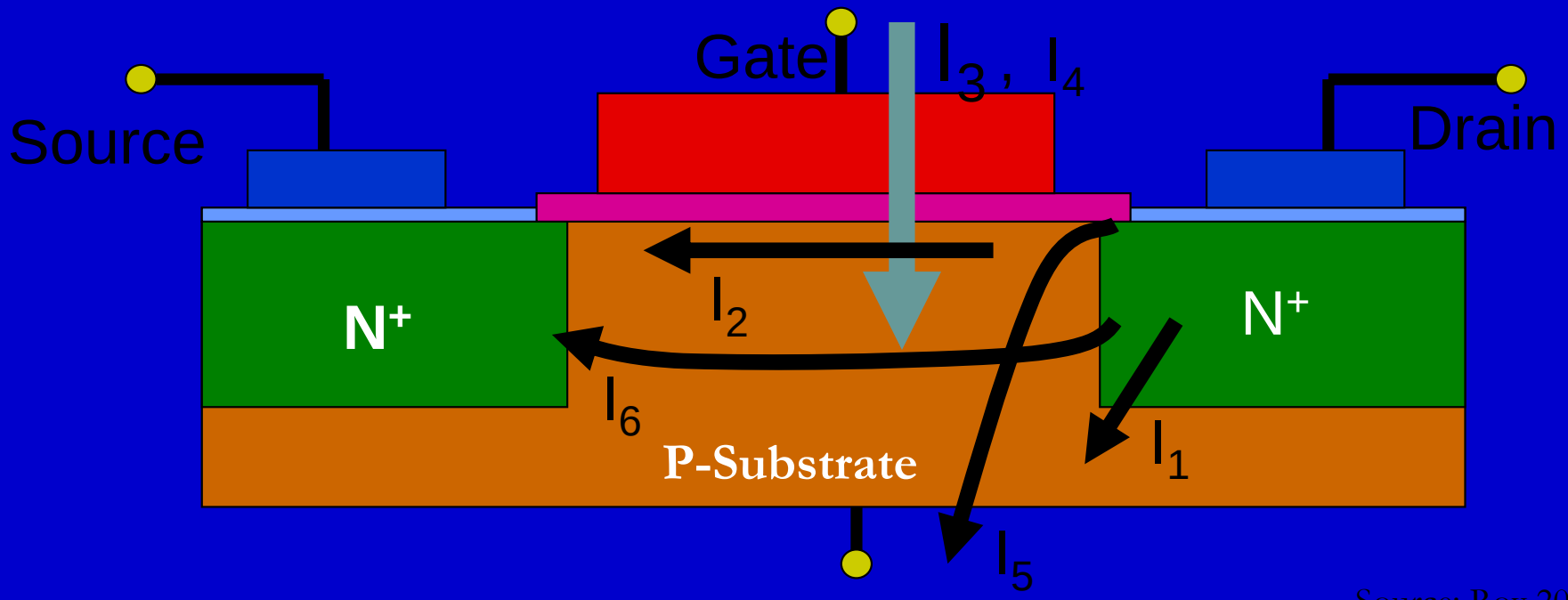
**Dynamic Dissipation**

- Capacitive Switching
- Tunneling current
- Short circuit

Source: Weste and Harris 2005

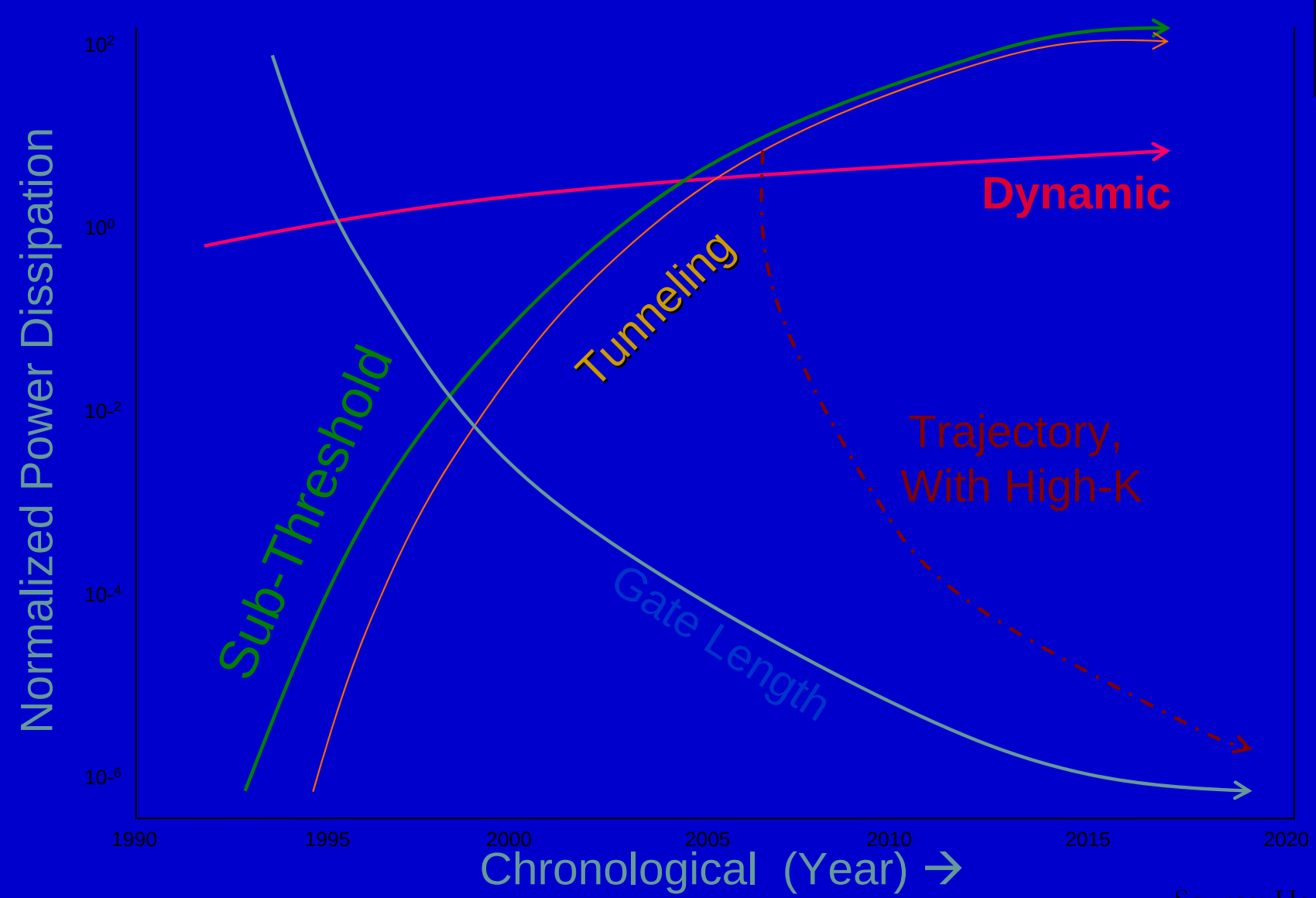
# Leakages in Nanometer CMOS

- ☑ $I_1$ : reverse bias pn junction (both ON & OFF)
- ☑ $I_2$ : subthreshold leakage (OFF )
- ☑ $I_3$ : oxide tunneling current (both ON & OFF)
- ☑ $I_4$ : gate current due to hot carrier injection (both ON & OFF)
- ☑ $I_5$ : gate induced drain leakage (OFF)
- ☑ $I_6$ : channel punch through current (OFF)



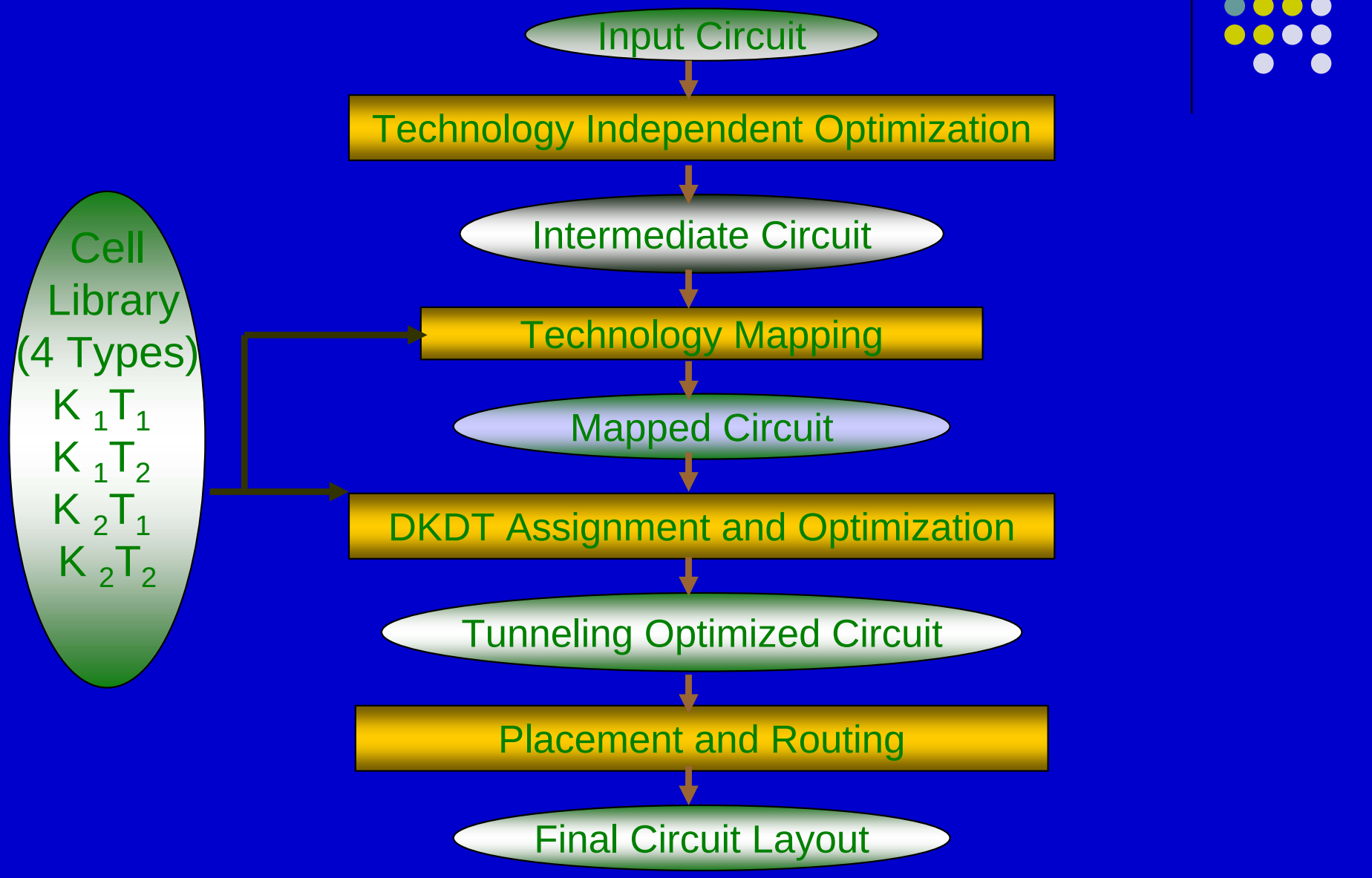

Source: Roy 2003

# Power Dissipation Trend

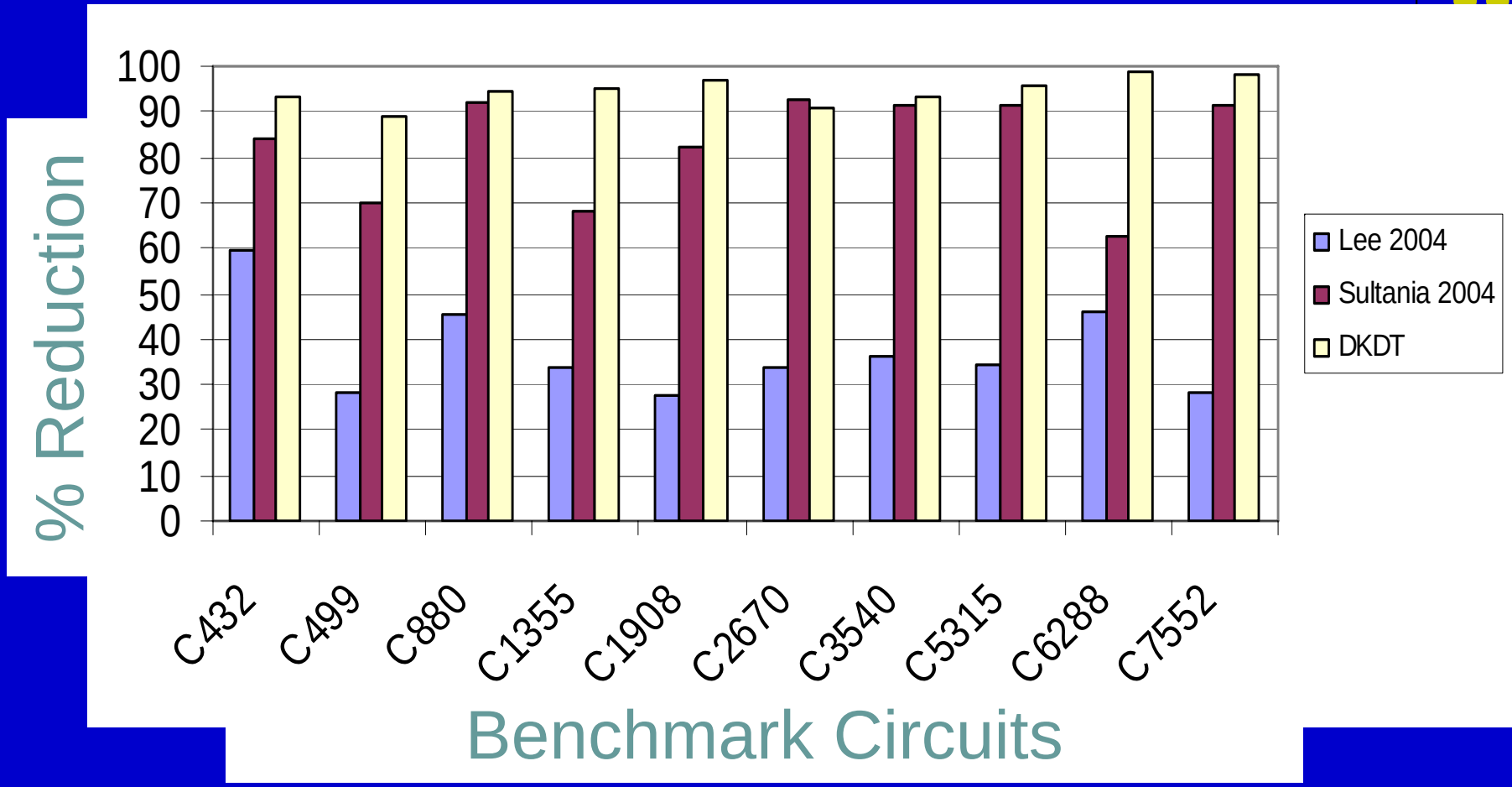



Source: Hansen 2004

# DKDT Based Logic Synthesis



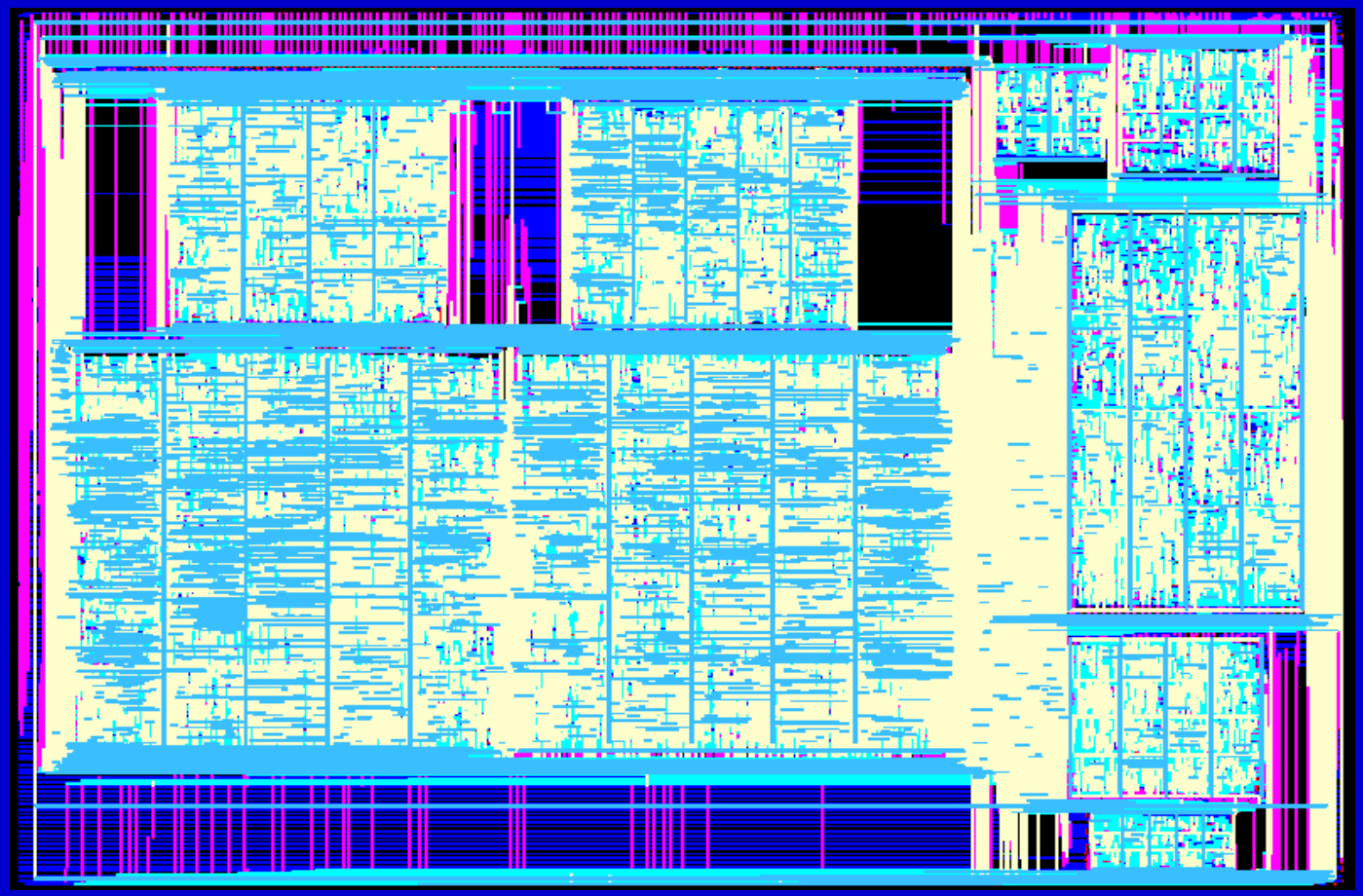
# DKDT Technique: Results



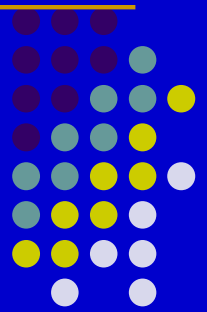

**NOTE**: DKDT has no time penalty.

# Facts about the latest chip designed

**(Claim: Lowest power consuming image watermarking chip available at present)**



# Chip: Statistics



**Technology: TSMC 0.25 µ**

**Total Area : 16.2 sq mm**

**Dual Clocks: 280 MHz and 70 MHz**

**Dual Voltages: 2.5V and 1.5V**

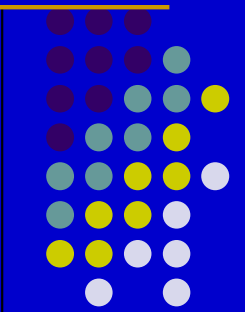
**No. of Transistors: 1.4 million**

**Power Consumption: 0.3 mW**


# Our Publication Statistics

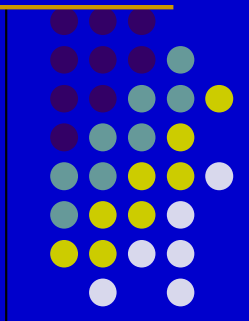
- Summary:
  - 6 ACM/IEEE transactions accepted and several in pipeline
  - 29 peer reviewed IEEE/ACM conference papers
- Selected List:
  - S. P. Mohanty and N. Ranganathan, “Simultaneous Peak and Average Power Minimization during Datapath Scheduling”, *IEEE Transactions on Circuits and Systems Part I (TCAS-I), Vol. 52, No. 6, June 2005, pp. 1157-1165*.
  - S. P. Mohanty and N. Ranganathan, “Energy Efficient Datapath Scheduling using Multiple Voltages and Dynamic Clocking”, *ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 10, No. 2, April 2005, pp. 330-353.*
  - S. P. Mohanty, N. Ranganathan, and R. K. Namballa, "A VLSI Architecture for Visible Watermarking in a Secure Still Digital Camera (S^2DC) Design", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 13, No. 7, July 2005, pp. 808-818.
  - S. P. Mohanty and N. Ranganathan, “A Framework for Energy and Transient Power Reduction during Behavioral Synthesis”, *IEEE Transactions on VLSI Systems (TVLSI)*, Vol. 12, No. 6, June 2004, pp. 562-572.

# Ph. D. in Computer Science



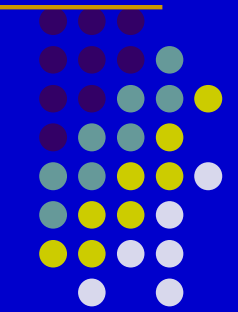
- Background or through course:
  - CMOS VLSI
  - VLSI CAD
  - Algorithms
  - Graph Theory
  - Optimization Techniques
  - Architecture
- Can focus on:
  - Any of the four research interests mentioned


# MS in Computer Science



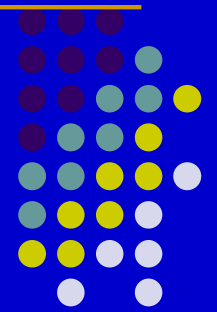
- Background or through course:
  - CMOS VLSI
  - VLSI CAD
  - Algorithms
  - Graph Theory
  - Optimization Techniques
- Can focus on:
  - CAD and Optimization for VLSI

# MS in Computer Engineering

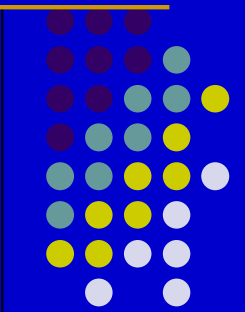


- Background or through course:
  - CMOS VLSI
  - Semiconductor Physics
  - Algorithms
  - Advanced VLSI Systems
- Can focus on:
  - Any of the four research interests mentioned

# Advantages of Thesis Option



- Less number of credit hours
- Chance of getting degree in 3 full semesters
- Chances of getting assistantship is higher
- Improves credibility of your masters degree
- Higher chances of getting better job
- More bargaining power for salary

# Thank You !!!