VLSI Design and CAD Laboratory

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Outline of the Talk

- About VDCL
- Current and Future Research
- Publications

VDCL

- Established in August 2004
- Mission:
  - to carry out research in low power VLSI design
  - to prepare next generation CAD tools for automatic design
- One Faculty and one student member and we are in the process of adding more members.
- Located at F231.
- Will have access to strong research infrastructure including Sun Fire server, Sun Workstations and Tera Bytes of storage all hooked through NFS with the help of new EE dept.
- Cadence, Synopsis, and Xilinx tools will be available.

Research Interests

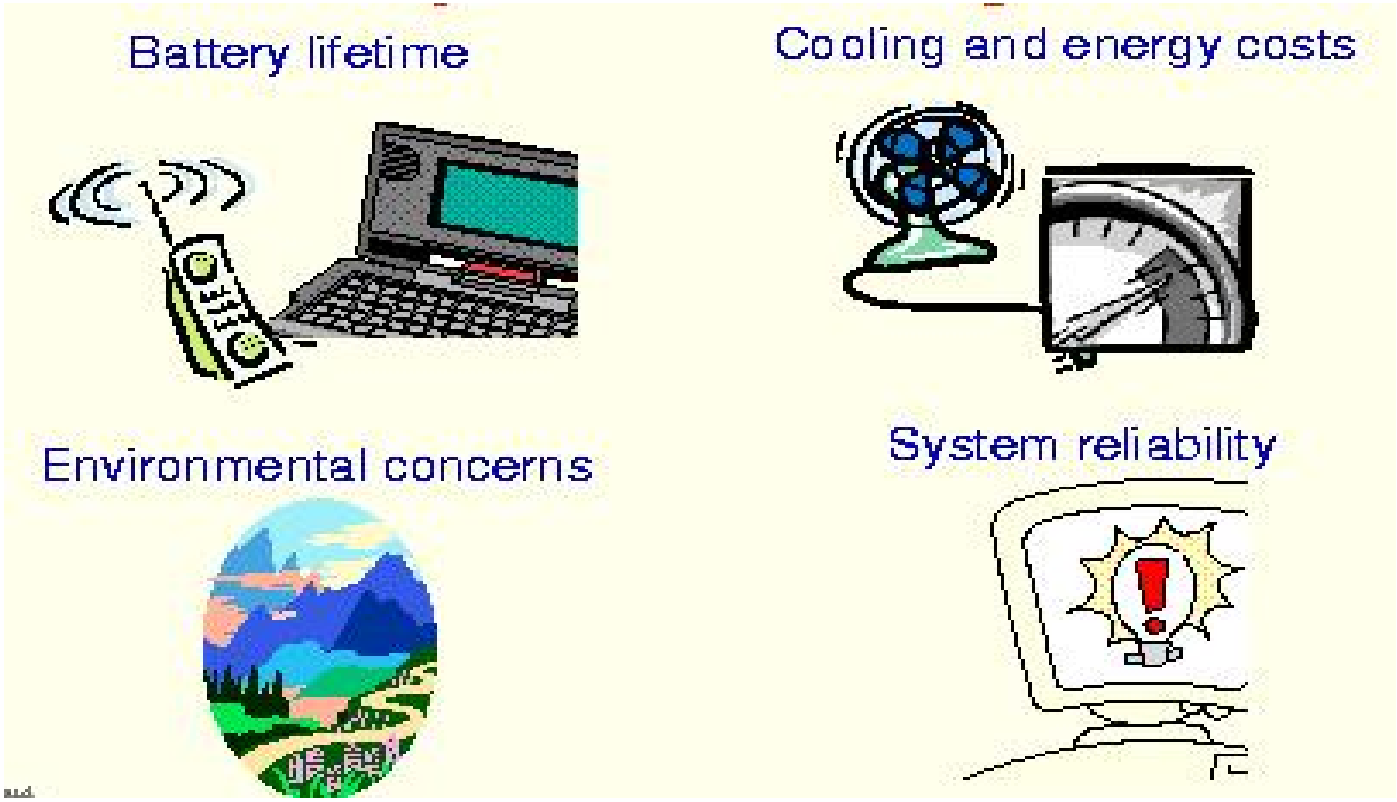
- CAD for Nanometer VLSI Circuits
- Low Power Synthesis
- Power Aware System Design
- High Level (Behavioral) Synthesis
- VLSI Signal Processing

Why Low-Power ?

Motivation: Extending battery life ……

Source: Internet

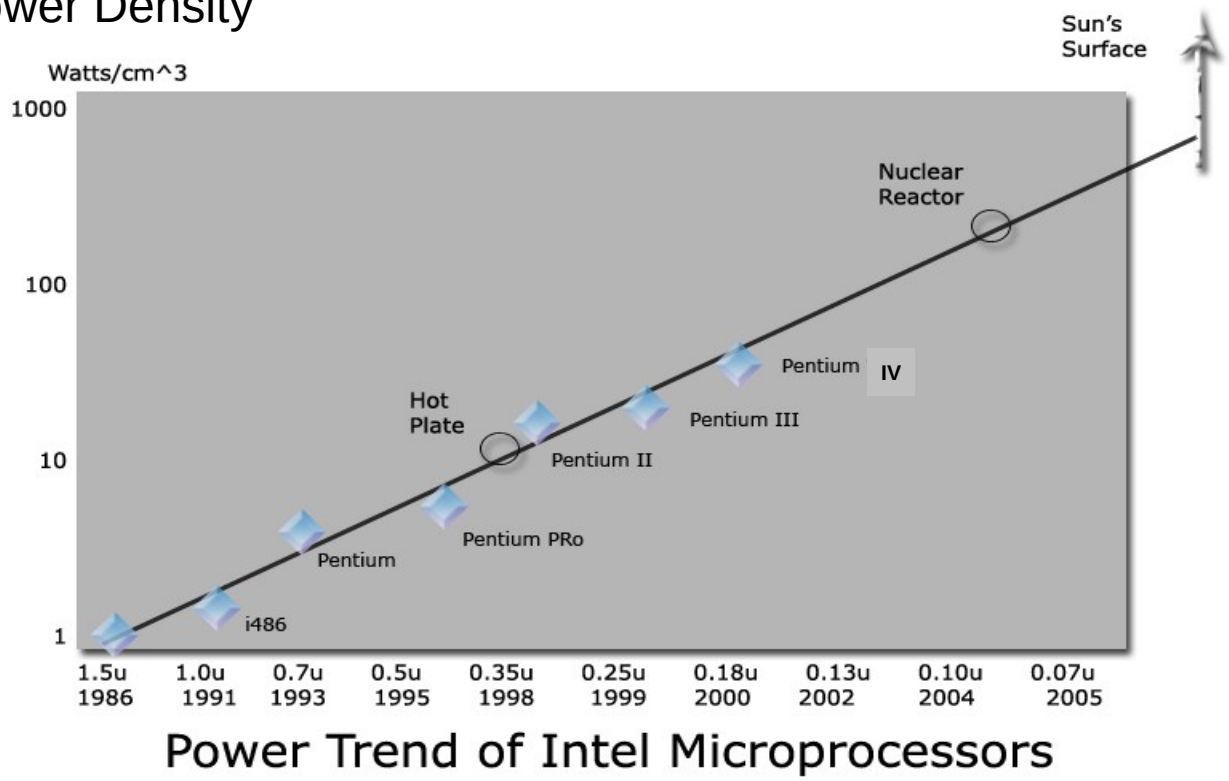
Why Low-Power ? ……..



Source: Internet

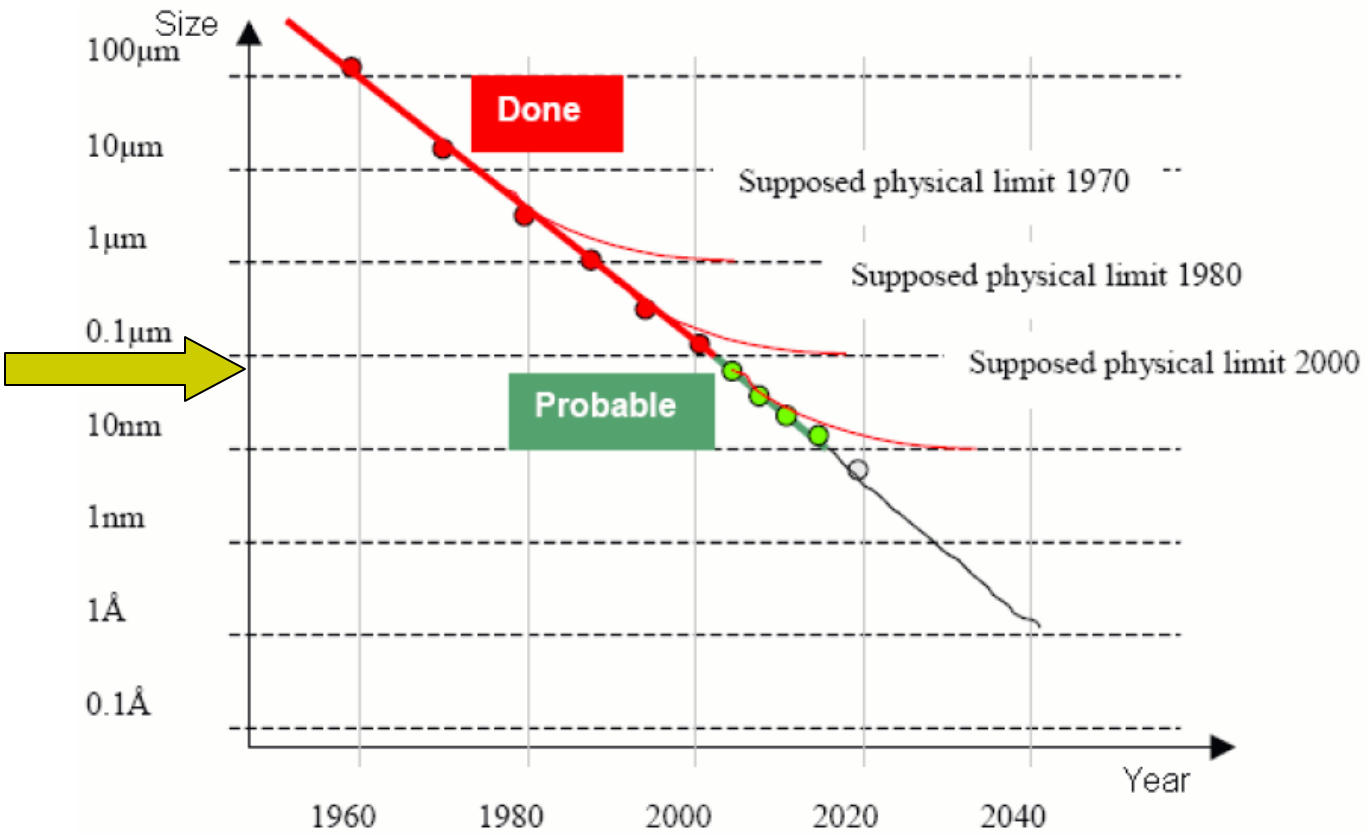
Why Low-Power ? ……..

Power Density



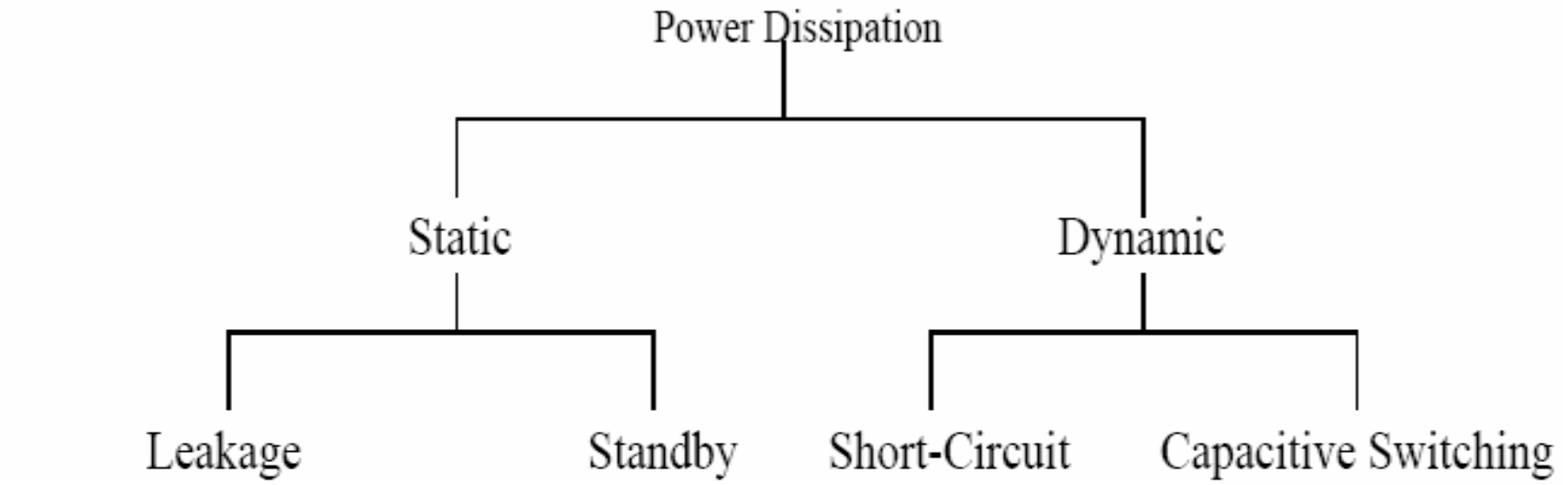
Power Trend of Intel Microprocessors

Technology Scaling Trend



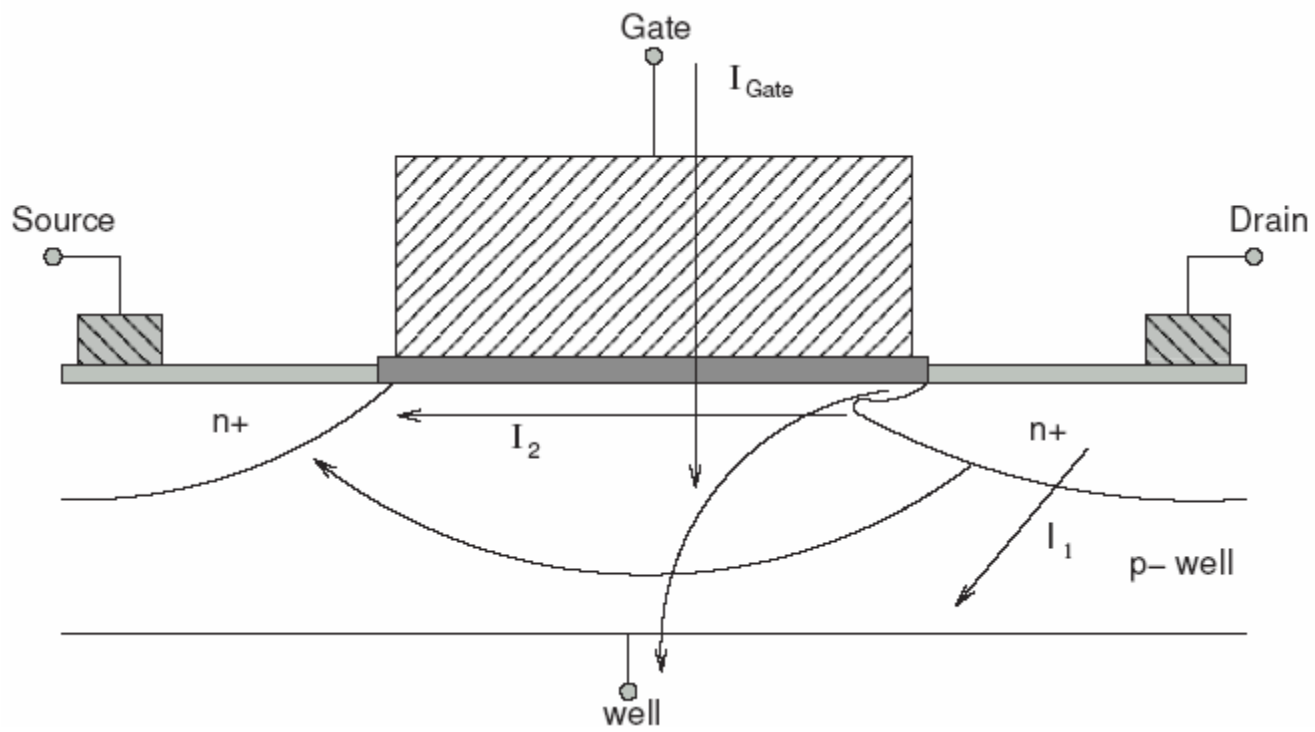
Source: Bendhia 2003

Power Dissipation in CMOS



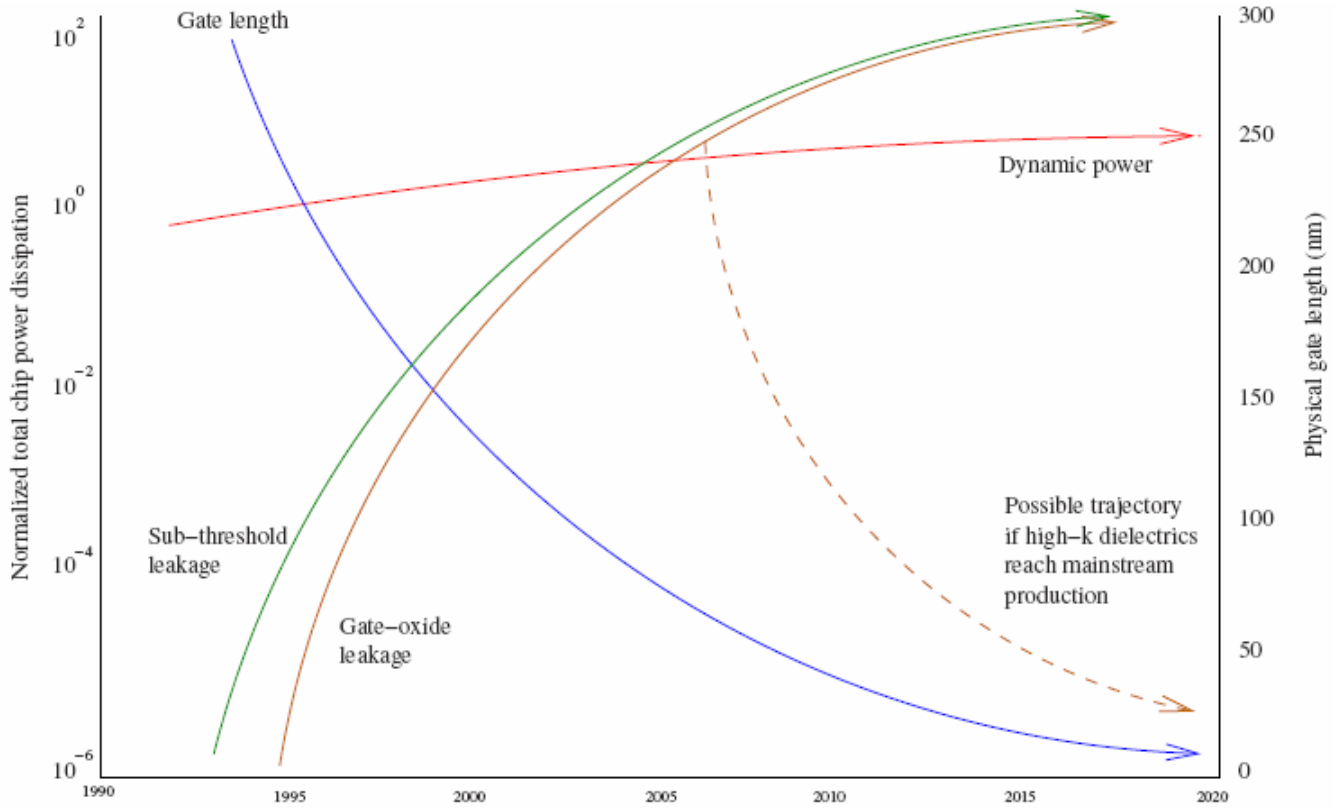
Source: Mohanty 2003

Leakage in Nanometer CMOS



Source: Roy 2003

Power Dissipation Trend

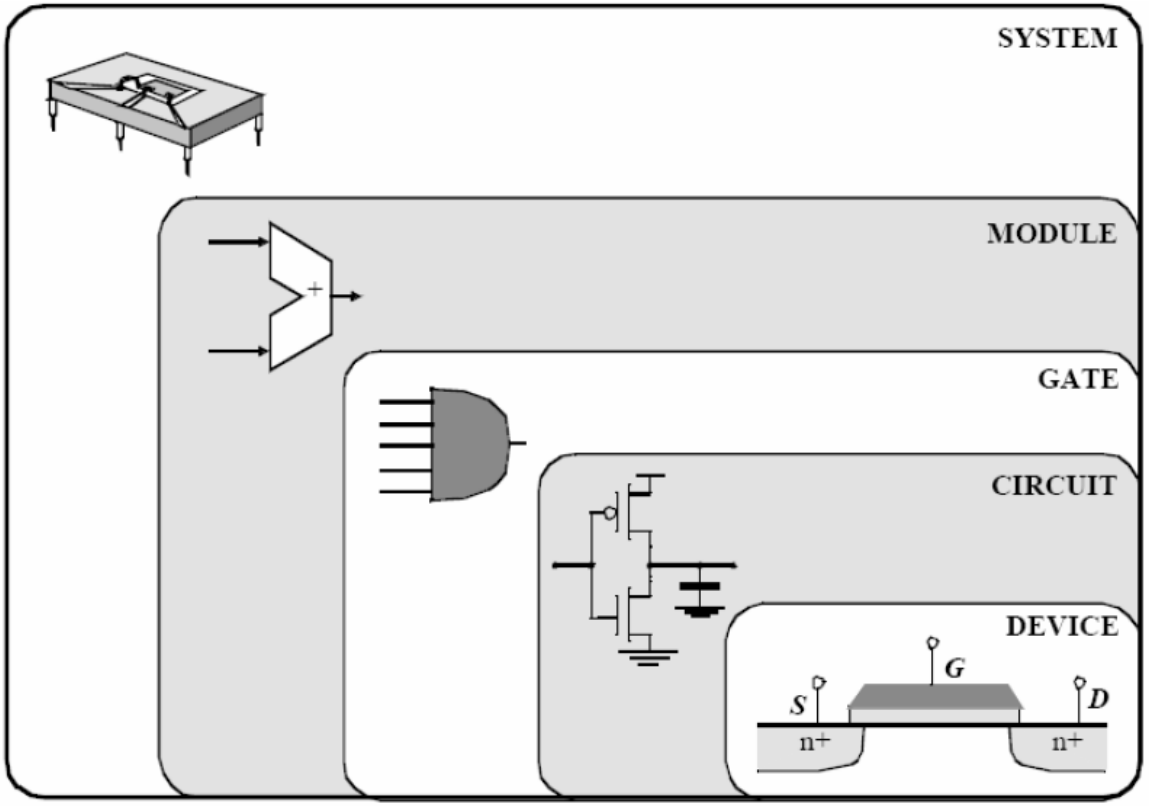


Source: Hansen 2004

For Dynamic Power Reduction?

Adjust the frequency and supply voltage in a co-coordinated manner to reduce dynamic power while maintaining performance.

Digital Circuits : Design Abstraction



Source: Rabaey 2003

Publications on Behavioral Synthesis

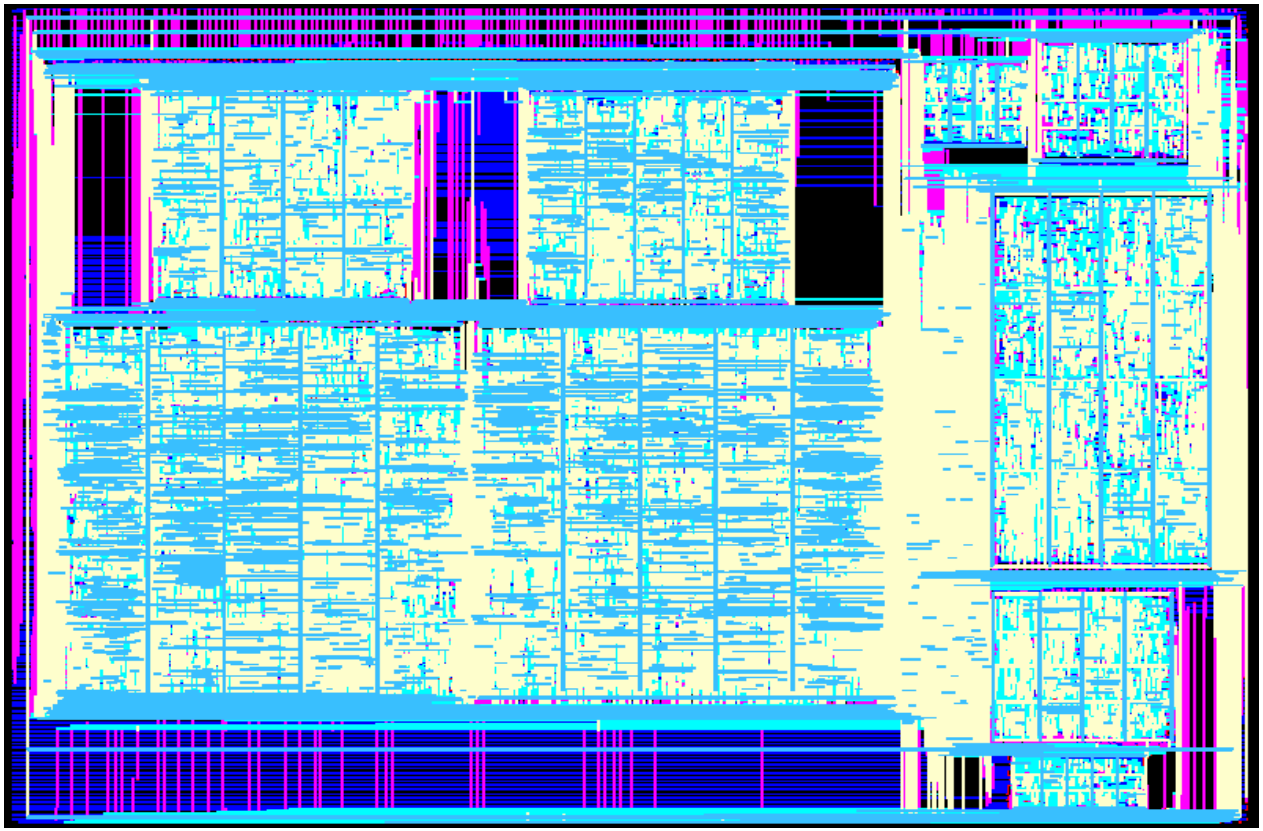
- Summary:
  - 4 ACM/IEEE transactions accepted and several in pipeline
  - 9 peer reviewed IEEE/ACM conference papers
- Selected List:
  - S. P. Mohanty and N. Ranganathan, "Simultaneous Peak and Average Power Minimization during Datapath Scheduling", Accepted in *IEEE Transactions on Circuits and Systems Part I (TCAS-I)*.
  - S. P. Mohanty and N. Ranganathan, "Energy Efficient Datapath Scheduling using Multiple Voltages and Dynamic Clocking", Accepted in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*.
  - S. P. Mohanty, N. Ranganathan, and S. K. Chappidi, "ILP Models for Simultaneous Energy and Transient Power Minimization during Behavioral Synthesis", Accepted in *ACM Transactions on Design Automation of Electronic Systems (TODAES)*.
  - S. P. Mohanty and N. Ranganathan, "A Framework for Energy and Transient Power Reduction during Behavioral Synthesis", *IEEE Transactions on VLSI Systems (TVLSI)*, Vol. 12, No. 6, June 2004, pp. 562-572.

Publications on VLSI Signal Processing

- Summary:
  - 2 IEEE transactions under review/revision
  - 5 peer reviewed ACM/IEEE conference papers and one peer reviewed paper in LNCS
- Selected List:
  - S. P. Mohanty, N. Ranganathan, and K. Balakrishnan, "A Dual Voltage Dual Frequency Low Power VLSI Chip for Image Watermarking", Revised and Resubmitted to *IEEE Transactions on Circuits and Systems Part I (TCAS-I)*.
  - S. P. Mohanty, N. Ranganathan, and K. Balakrishnan, "Design of a Low Power Image Watermarking Encoder using Dual Voltage and Frequency", Accepted in the *Proceedings of the 18th IEEE International Conference on VLSI Design (VLSID)*, 2005.
  - S. P. Mohanty, N. Ranganathan, and R. K. Namballa, "A VLSI Architecture for Visible Watermarking in a Secure Still Digital Camera Design", Submitted to *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*.
  - S. P. Mohanty, R. Kumara C., and S. Nayak, "FPGA Based Implementation of an Invisible-Robust Image Watermarking Encoder", *Lecture Notes in Computer Science (LNCS), CIT 2004*, Springer-Verlag, Vol. 3356, pp. 344-353, 2004.
  - S. P. Mohanty, N. Ranganathan and R. K. Namballa, "VLSI Implementation of Visible Watermarking for a Secure Digital Still Camera Design", in *Proceedings of the 17th IEEE International Conference on VLSI Design (VLSID)*, pp. 1063-1068, 2004.

Facts about the latest chip designed

(Claim: Lowest power consuming image watermarking chip available at present)



Chip: Statistics

Technology: TSMC 0.25 µ

Total Area : 16.2 sq mm

Dual Clocks: 280 MHz and 70 MHz

Dual Voltages: 2.5V and 1.5V

No. of Transistors: 1.4 million

Power Consumption: 0.3 mW

Thank You !!!