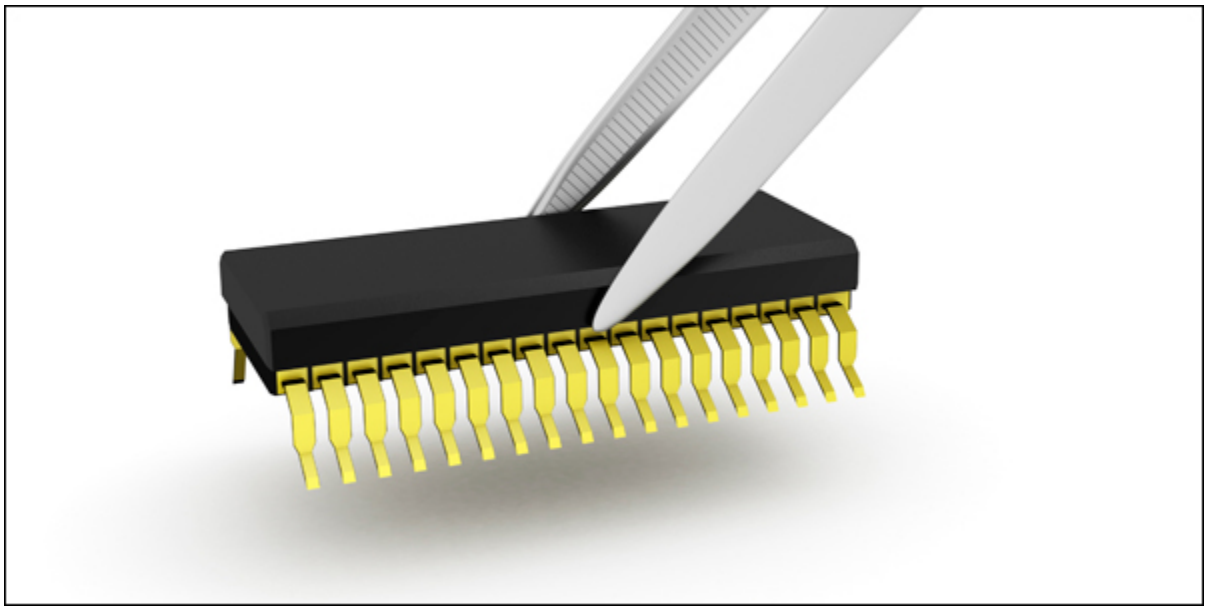
Longer battery life for the devices we love

Posted on December 21st, 2010, by admin



More Battery Life with Less Power

Researchers at the University of North Texas are leading the charge to reduce the time your electronic devices spend on the charger.

With minimal use, portable systems, like mobile phones, will last 10 hours on one charge. But more than likely you'll have to replenish the battery in a few hours. Power leakage and inefficient consumption have long been a problem Dr. Saraju Mohanty hopes to solve.

Mohanty, associate professor of computer science and engineering at the University of North Texas and director of UNT's Nanosystem Design Laboratory has, during the past five years, developed innovative methods to estimate and optimize the energy efficiency of nanoscale circuits during their design phase.

These chips contains hundreds of millions of "switches" that are smaller than the width of a human hair. Typically, measuring the chip's performance occurs during the manufacturing process, but Mohanty uses high-end computer equipment to simulate and model the chip's propensity to leak power and to identify possible design improvements.

Plugging the leaks

"If we manufacture the chip and we decide we do not like it because the power is not good, then our money is wasted," says Mohanty. "My research is answering the question 'how do we predict, how do we estimate

how good it will be in terms of power during the design phase?' It is a difficult thing because we don't have the chip."

The more efficient the chip's design, the less power it will use or leak, resulting in less charging. Since batteries are charged using electricity sources, reducing the frequency of charger time translates to enhanced conservation. Multiply that several million times and it could mean big savings.

With computer-aided design (CAD) simulations, Mohanty can predict within a 5 percent margin how much power the chip will consume. His research centers on the power consumption of very-large-scale integration (VLSI) chips otherwise known as microprocessors.

"We have a lot of techniques where we can reduce the power consumption of the chip by 90 percent," Mohanty says.

From Texas to the world

Mohanty's research has received close to $1 million from the National Science Foundation (NSF) and from the Semiconductor Research Corporation to fund student research assistants and purchase two high-end computer systems and servers. The equipment gives students a chance to learn how to run simulations that manufacturers need to improve their products.

In May, Mohanty's group received a $90,000 grant from the NSF to develop a simulation-based curriculum to further develop a nanotechnology track for undergraduate engineering programs. That track would include three courses that will advance nanoelectronics education.

In August 2009, Mohanty received nearly $250,000 in American Recovery and Reinvestment Act Funds from the NSF to purchase equipment that would conduct nanoscale circuit modeling including a high-end, 4-processor server with 16-GB local memory and 4-TB RAID5 storage to be used by two faculty members and 10 students for nanoscale data management. The funds also supported under-represented students for their research.

As a result of Mohanty's research, he receives guidance on devices still in development from industrial collaborators. He runs them through the modeling process that ultimately can produce more efficient, lower priced products for consumers.

In addition to his research and education at UNT, Mohanty is organizing the International Symposium on Electronic System Design 2010 in December in Bhubaneswar, India. The symposium will bring together representatives from organizations that develop the five main components of the cell phone.

"This technology is my hobby," he says, "I keep track of things, what is going on and what people want in the future in the consumer market."

- *Tracey Lamphere*

Share and Enjoy:

Tags: EDUCATION, ENERGY, ENGINEERING, RESEARCH