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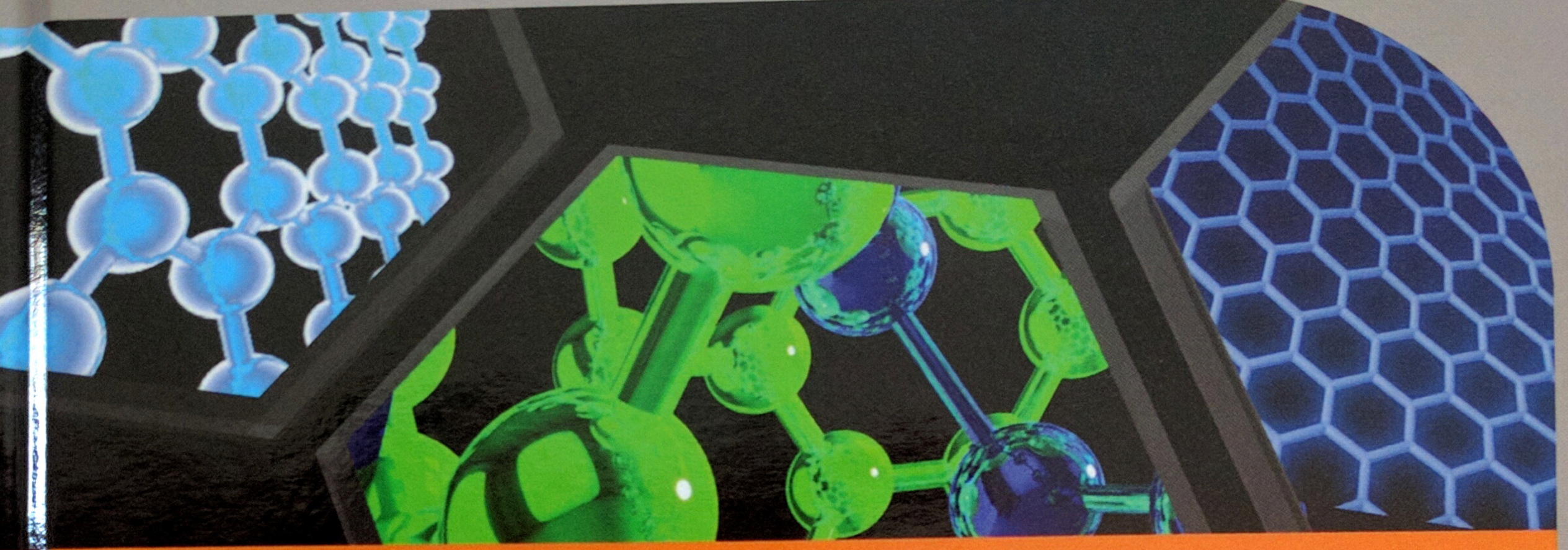

Nano-CMOS and Post-CMOS Electronics: Circuits and Design

Edited by
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SPICEless RTL Design Optimization of Nanoelectronic Digital Integrated Circuits

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The previous chapter discussed various steps of high-level synthesis (HLS) which are used for design exploration of digital integrated circuits. It then discussed specific methods for dynamic power dissipation optimization as well as synthesis of hardware-trojan free digital integrated circuits. The methods relied on various bio-inspired algorithms for design space exploration. As complementary material of the previous chapter, this chapter presents HLS methods for leakage-optimal digital integrated circuit design exploration. Specifically, a paradigm shift approach is presented in which the complete HLS flow is performed without use of any electronic design automation (EDA) tool. All the associated tasks such as modeling, characterization, and optimization, are performed using non-EDA tools and hence this is called the "SPICEless" approach. For a specific objective of nanoelectronic digital integrated circuits, gate-leakage power dissipation is targeted.

1 Introduction

Application specific circuits and systems for various requirements involving digital signal processing (DSP) are everywhere. DSP chips are part of media players, DVD players, bluray players, smart mobile phones, tablets, digital TVs, etc. These electronic systems a have profound impact on society and are used continuously throughout the globe (refer Fig. 1). Application specific circuits and systems are quite complex in terms of transistor count due to the need of high-throughput that involves a very large number of operations per unit time. Such application specific circuits and systems (also referred as application specific systems-on-chip) have stringent power budget to reduce energy consumption as well as specific needs for battery operated portable electronics [29, 30]. Complex digital integrated circuits are primarily fabricated using nanoscale complementary metal-oxide semiconductor (nano-CMOS) processes, a specific example of nanoelectronic technology. Nanoelectronic technology has made it possible to fabricate complex integrated circuit in limited silicon areas. However, the use of nanoelectronic technology has made design iterations to achieve closure numerous as well as more effort intense as far as design engineers are conserned. The use of nanolectronic technology also has changed the power dissipation components present in the overall power profile of individual devices and overall circuits or systems [31].

The design flows of complex digital circuits and systems use a divide and conquer approach in which the circuit or system is represented by various abstraction levels such as system level and architecture level. Design engineers work at a specific level of design abstraction using tools needed at that level and perform the design using the components present at a specific level. For example, at the architecture level datapath components such as adders and multipliers can be used for design exploration of the application specific integrated circuit. At this level, digital hardware description languages such as VHDL and SystemVerilog can be used [29, 30]. A specific example of automated design approach which is used at the architecture level is high-level synthesis (HLS) [32, 45, 35, 30, 27]. The outcome of HLS is a register-transfer level (RTL) structure or a target architecture of the digital integrated circuit consisting of a datapath and controller. The three major steps of HLS consist of scheduling, allocation, and binding. Any optimization conducted during these HLS phases leads to an optimal RTL structure or RTL description. Depending on the datapath component library available, algorithms used for the HLS stages and constraints, different optimizations can be performed to obtain optimal RTL descriptions or architecture-level descriptions. Thus, HLS phase optimization, RTL optimization, and architecture-level optimization are used interchangeably. The previous chapter presented the basic steps of

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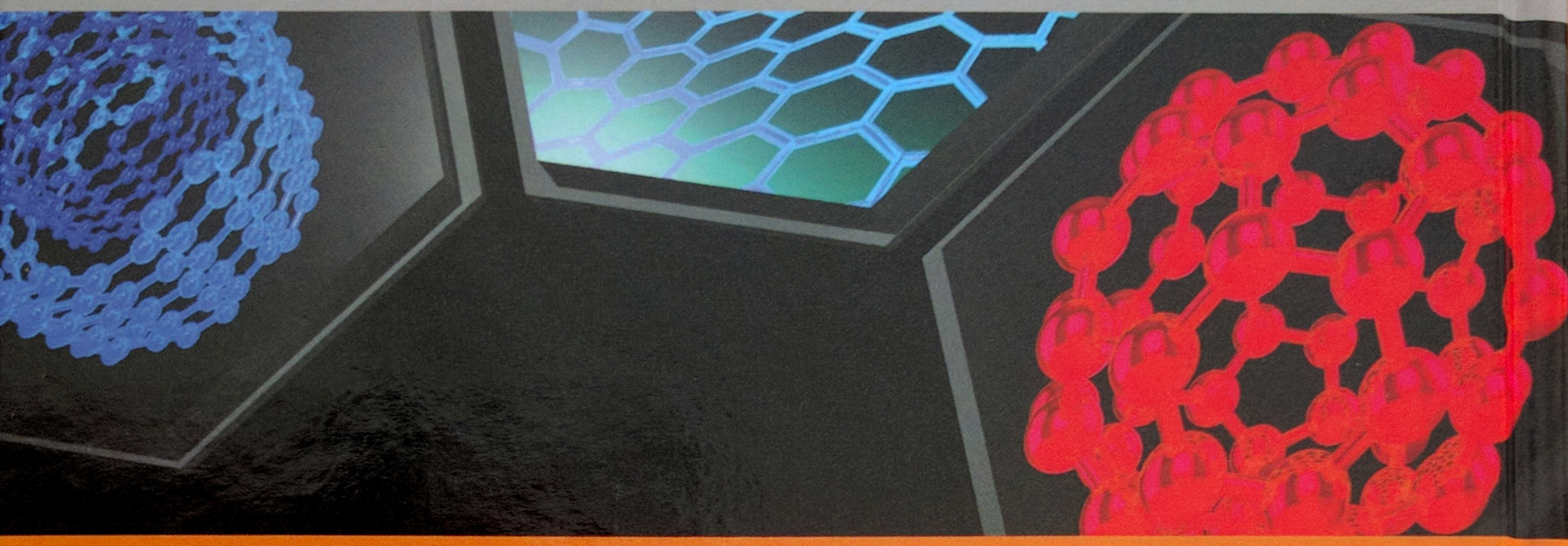

Nano-CMOS and Post-CMOS Electronics: Circuits and Design

The demand for ever smaller and portable electronic devices has driven metal oxide semiconductor-based (CMOS) technology to its physical limit with the smallest possible feature sizes. This presents various size-related problems such as high power leakage, low-reliability, and thermal effects, and is a limit on further miniaturization. To enable even smaller electronics, various nanodevices including carbon nanotube transistors, graphene transistors, tunnel transistors and memristors (collectively called post-CMOS devices) are emerging that could replace the traditional and ubiquitous silicon transistor. This book explores these nanoelectronics at the circuit and systems levels including modelling and design approaches and issues.

Topics covered include self-healing analog and radio frequency circuits; on-chip gate delay variability measurement in scaled technology node; nanoscale finFET devices for PVT aware SRAM; data stability and write ability enhancement techniques for finFET SRAM circuits; low-leakage techniques for nanoscale CMOS circuits; thermal effects in carbon nanotube VLSI interconnects; lumped electro-thermal modeling and analysis of carbon nanotube interconnects; high-level synthesis of digital integrated circuits in the nanoscale mobile electronics era; SPICEless RTL design optimization of nanoelectronic digital integrated circuits; green on-chip inductors for three-dimensional integrated circuits; 3D network-on-chips; and DNA computing.

This book is essential reading for researchers, research-focused industry designers/developers, and advanced students working on next-generation electronic devices and circuits.

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