

Nano-CMOS

and Post-CMOS Electronics: Circuits and Design

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High-Level Synthesis of Digital Integrated Circuits in the Nanoscale Mobile Electronics Era

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I. INTRODUCTION

The impact of consumer electronics such as mobile phones, digital cameras, digital television, and DVD/MP3 players is profound on our society. The central module of these products is a miniature size integrated circuit (IC) which finds wide spectrum applicability from kitchen appliances, to automobiles, to aircrafts or to any embedded systems. The system in these aforesaid modern consumer electronics products is built as an Analog/Mixed-Signal System-on-chip (AMS-SoC) [45] where the digital circuits are the main computational modules while the analog or mixed-signal components are interfacing circuits, in a typical case. Therefore, proficient design of digital ICs has become the need of the hour as it serves as one of the significant driving factors of efficient system design in this current mobile electronics era (the various factors such as speed, power, reliability etc involved during design of handheld devices is as shown in Fig. 1). The complexity of digital ICs in terms of number/size of transistors is quite large. However, the digital ICs have well-defined designs of abstractions such as system, algorithm, register transfer, and logic which through the application of divide and conquer approach can be exploited to handle the complex digital IC design flow. Each design abstraction layer has its own corresponding automated design methods or computer-aided design (CAD) methods which enables design of error free ICs within acceptable design time. One such automatic CAD technique is high-level synthesis (also known as behavioral, architectural, or algorithmic synthesis), which comprises of design space exploration process that allows exploration of design alternatives yielding to an optimized design option, prior to layout of the circuit in actual silicon. High-level synthesis (HLS) is defined as the translation of a behavioral description to a structural description, i.e., from behavioral hardware description languages like VHDL, Verilog, SystemVerilog, to register-transfer level VHDL and Verilog [14].

As discussed above, high level synthesis is the transition of an application, represented through a control data flow graph(CDFG), from its system or algorithmic level description to the equivalent register transfer level (RTL) counterpart while

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Nano-CMOS and Post-CMOS Electronics: Circuits and Design

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The demand for ever smaller and portable electronic devices has driven metal oxide semiconductor-based (CMOS) technology to its physical limit with the smallest possible feature sizes. This presents various size-related problems such as high power leakage, low-reliability, and thermal effects, and is a limit on further miniaturization. To enable even smaller electronics, various nanodevices including carbon nanotube transistors, graphene transistors, tunnel transistors and memristors (collectively called post-CMOS devices) are emerging that could replace the traditional and ubiquitous silicon transistor. This book explores these nanoelectronics at the circuit and systems levels including modelling and design approaches and issues.

Topics covered include self-healing analog and radio frequency circuits; on-chip gate delay-variability measurement in scaled technology node; nanoscale finFET devices for PVT aware SRAM; data stability and write ability enhancement techniques for finFET SRAM circuits; low-leakage techniques for nanoscale CMOS circuits; thermal effects in carbon nanotube VLSI interconnects; lumped electro-thermal modeling and analysis of carbon nanotube interconnects; high-level synthesis of digital integrated circuits in the nanoscale mobile electronics era; SPICEless RTL design optimization of nanoelectronic digital integrated circuits; green on-chip inductors for threedimensional integrated circuits; 3D network-on-chips; and DNA computing. This book is essential reading for researchers, research-focused industry designers/developers, and advanced students working on next-generation electronic devices and circuits. **Saraju Mohanty** is Professor at the Department of Computer Science and Engineering, University of North Texas, where he is the director of NanoSystem Design Laboratory (NSDL). His research interests focus on Energy-Efficient High-Performance Secure Electronic Systems. He is the author of more than 200 peer-reviewed journal and conference publications and 3 books. Prof. Mohanty is the current Chair of Technical Committee on Very Large Scale Integration (TCVLSI) of the IEEE Computer Society, is on the editorial board of IET Circuits, Devices and Systems, Integration and Journal of Low Power Electronics, and serves on the organizing and program committee of several international conferences.

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