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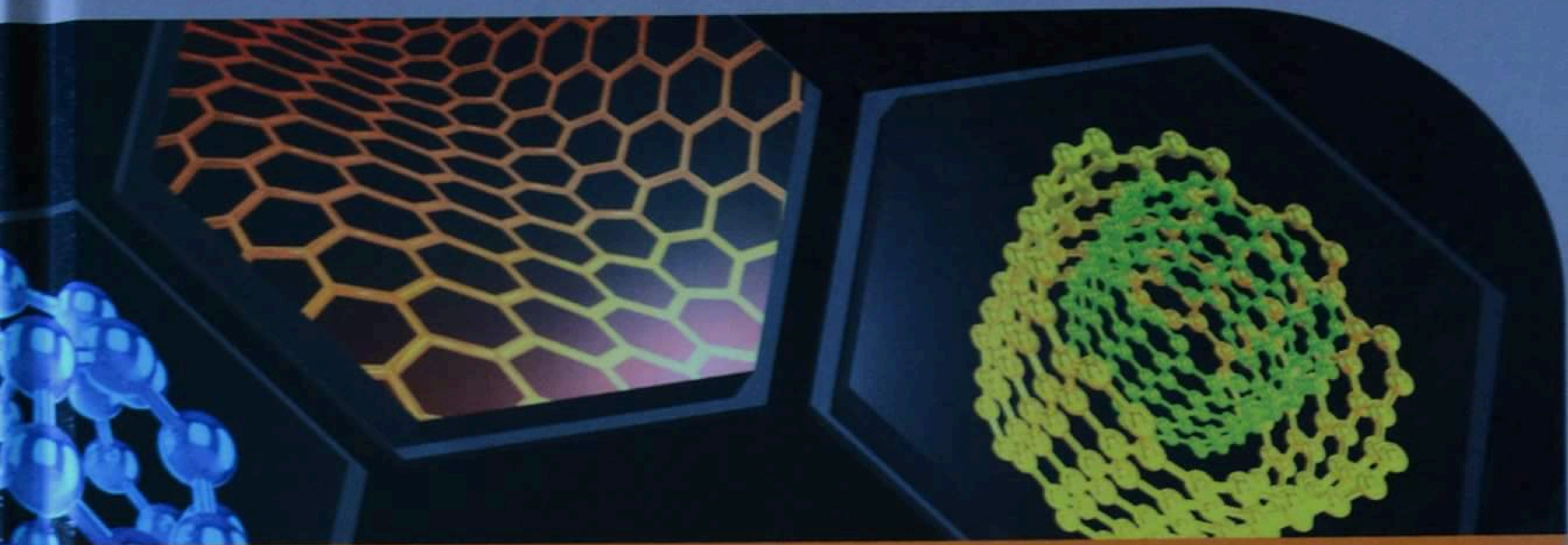

Nano-CMOS and Post-CMOS Electronics: Devices and Modelling

Edited by
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Nanoscale High-κ/Metal-Gate CMOS and FinFET based Logic Libraries

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During the last four decades, VLSI technology growth has been driven by miniaturization that reduces cost per transistor, power consumption per transistor, with higher packing density and reduced cost of operation. However, the small transistor size leads to very high electric fields across the gate oxide which causes the difficult problem of gate oxide leakage. This problem is mitigated by high-κ/metal-gate technology, in which the gate material is copper (*going back to metal from polysilicon*) and the gate oxide material is a not silicon dioxide. At the same time, explosive growth of mobile portable electronics has been the driver for many scientific, engineering, and technological breakthroughs in the last few decades. Mobile electronics in particular, such as smart mobile phones, spend most of their operational time in waiting for a call or similar event. However, during these wait states leakage power dissipation has been a major issue since it drains the battery continuously. The industry has explored various solutions to reduce the OFF state leakage and multiple gate devices emerged as a solution to this problem. Double gate FinFET technology is considered as a solution to reduce OFF state leakage while having faster ON and OFF transitions and low-power dissipation. This chapter discusses these devices and presents logic libraries which can be used in the digital synthesis of large integrated circuits using such devices through electronic design automation (EDA) tools.

1 Introduction

The growth of VLSI technology is one of the fastest observed in human history. This has been made possible by several milestone inventions. Initially, metal-oxide semiconductor field effect transistors (MOSFETs) had aluminum gates which were slow, large in area, unreliable, with high leakage currents. Then a self-aligned-gate process arrived in which the gates of the transistors were made with polycrystalline silicon [60], *not a metal*. The scaling of CMOS technology has accelerated in recent years and will arguably continue toward the 8 nm regime [4]. The superior properties of SiO_2 permit the fabrication of properly functioning devices with SiO_2 layers as thin as 1.5 nm. Further scaling of the SiO_2 layer thickness leads to tunneling gate leakage [4, 37, 52]. In addition, the small transistor size leads to very high electric fields across the gate oxide which causes the difficult problem of gate oxide leakage [41]. The use of ultra-low thickness gate oxide for short channel transistors presents the problem of gate oxide leakage in its ON, OFF, and transition states. These problems are mitigated by high-κ/metal-gate technology, in which the gate material is copper (*going back to metal from polysilicon*) and the gate oxide is a not silicon dioxide [7]. An insulator with a higher dielectric constant κ than that of SiO_2 ($= 3.9$) is used. Statistical characterization of high-κ/metal-gate digital gates as a function of process parameter variation is needed for design. In this chapter, a methodology is presented for PVT-aware high-κ/metal-gate logic library characterization. The methodology considers the process variation effects of 15 device parameters. First, statistical models for gate-induced-drain leakage (GIDL) current ($\hat{I}_{GIDL}$), off-current ($\hat{I}_{OFF}$) and drive current ($\hat{I}_{ON}$) are presented at device level. This is followed by statistical characterization of the library logic cells at room temperature. Statistical results for subthreshold current ($\hat{I}_{sub}$), GIDL current, dynamic current ($\hat{I}_{dyn}$) and delay are derived. This is followed by results for PVT-aware characterization of logic cells. The library can be used by circuit designers for digital synthesis and design exploration.

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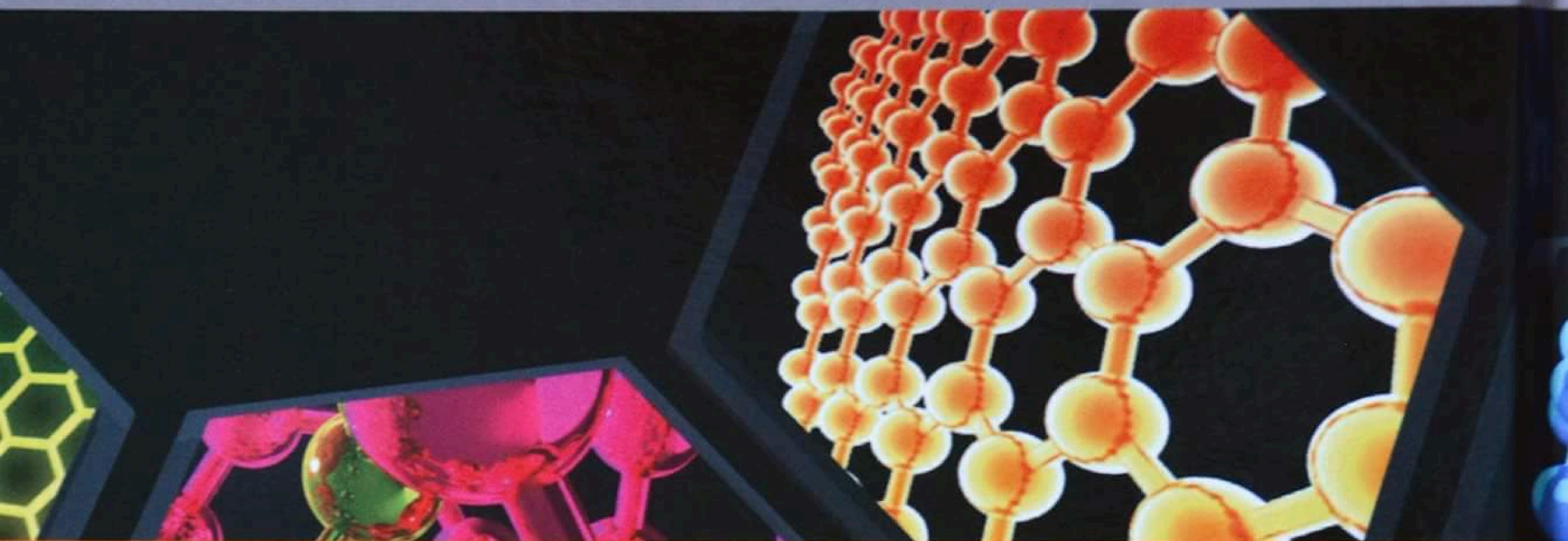

Nano-CMOS and Post-CMOS Electronics: Devices and Modelling

The demand for ever smaller and portable electronic devices has driven metal oxide semiconductor-based (CMOS) technology to its physical limit with the smallest possible feature sizes. This presents various size-related problems such as high power leakage, low-reliability, and thermal effects, and is a limit on further miniaturization. To enable even smaller electronics, various nanodevices including carbon nanotube transistors, graphene transistors, tunnel transistors and memristors (collectively called post-CMOS devices) are emerging that could replace the traditional and ubiquitous silicon transistor. This book explores these nanoelectronics at the device level including modelling and design.

Topics covered include high-k dielectrics; high mobility n and p channels on gallium arsenide and silicon substrates using interfacial misfit dislocation arrays; anodic metal-insulator-metal (MIM) capacitors; graphene transistors; junction and doping free transistors; nanoscale gigh-k/metal-gate CMOS and FinFET based logic libraries; multiple-independent-gate nanowire transistors; carbon nanotubes for efficient power delivery; timing driven buffer insertion for carbon nanotube interconnects; memristor modeling; and neuromorphic devices and circuits.

This book is essential reading for researchers, research-focused industry designers/developers, and advanced students working on next-generation electronic devices and circuits.

Saraju Mohanty is Professor at the Department of Computer Science and Engineering, University of North Texas, where he is the director of NanoSystem Design Laboratory (NSDL). His research interests focus on Energy-Efficient High-Performance Secure Electronic Systems. Prof. Mohanty is an inventor of 4 US patents, and an author of 200 peer-reviewed articles and 3 books. Prof. Mohanty is the current Chair of Technical Committee on Very Large Scale Integration (TCVLSI) of the IEEE Computer Society, is on the editorial board of IET Circuits, Devices and Systems, Integration and Journal of Low Power Electronics, and serves on the organizing and program committee of several international conferences.

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