Nanoelectronic Mixed-Signal System Design

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Mc Graw Hill Education

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Chapter 1
Opportunities and Challenges of Nanoscale Technology and Systems

1 Introduction

Consumer electronics such as mobile phones, digital cameras, digital television, high-definition content players, health monitoring systems, and DVD/MP3 players have profound impact on society. The main component of these appliances is a tiny integrated circuit (IC) [141, 37, 43]. ICs are everywhere, from kitchen appliances, to automobiles, to aircrafts. A system in modern consumer electronics is built as an Analog/Mixed-Signal System-on-chip (AMS-SoC) [43, 72, 85, 61, 17]. A representative AMS-SoC is illustrated in Fig. 1. It has image sensors for the camera. General purpose digital processor is programmable and executes the system and application softwares. Digital signal processor (DSP) performs the signal processing in the system. Analog circuits are absolutely necessary in AMS-SoCs at least as interface elements even when the functions are being performed by digital processors. In a smartphone, the baseband telecommunication chip perform the communication operations using GSM or CDMA protocols. It is the main chipset of the smartphones and directly interfaced to other hardware like speakers. The wireless operation and bluetooth connects are taken care of the wireless component. Data converter sircuits like analog-to-digital- converters (ADCs) and digital-analog-converters (DACs) are two intrinsic mixed-signal circuits [70, 127, 18]. For the portable electronic system a battery preferable rechargeable battery is included.

The hardware components of the present day AMS-SoCs are of gigascale complexity and consist of transistors of nanoscale process technology. The situation is depicted in Fig. 2. Nanoscale CMOS technology such as classical silicon-dioxide/polysilicon bulk MOSFET and high-κ/metal-gate MOSFET are used to build such hardwares. Triple gate transistors are With the growth of nanotechnology, a number of nanodevices have emerged to replace the classical MOSFET. Representative nanodevices include tri-gate field effect transistors (TGFETs) and graphene FET (GFET) [35, 40, 147]. The TGFET is being adopted for ultra-low-power designs. The GFET can operate at high-frequencies (e.g. 100 GHz) and has potential for high-speed nanoelectronics. Nanoscale size has reduced power dissipation of each

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Chapter 2
Emerging Systems Designed as Analog / Mixed-Signal System-on-Chips (AMS-SoCs)

1 Introduction

Due to ever decreasing cost of electronics hardware and softwares in last several years more and more people are able to afford to buy consumer electronics systems. The consumer electronics system have profound effects on the society. The transfer of information around the globe is possible in no time and without any cost. People around the globe are staying connected every moment through the social networks. This chapter discusses some example systems that has been used in day-to-day life or being conceptualized for future development. It is difficult to discuss all of these systems in the limited space. Attempt has been made to discuss a very selecting of them. The examples include systems that has been used in day-to-day life or being conceptualized for future development. The example system include the following: Biosensor Systems, Tablet PC, Smart Mobile Phone, Blue Ray Player, Multimedia Tank, TV Tuner Card, Secure Digital Camera (SDC), Net-Centric Multimedia Processor (NMP), Drug-Delivery Nano-Electro-Mechanical Systems (DDNEMS), Radio Frequency Universal Remote Control, Radio Frequency Identification (RFID) Tag, and Global Positioning System (GPS). These are typically designed as AMS-SoCs containing analog, digital, and RF circuits, FPGA, firmware, and software components.

2 Atomic Force Microscope (AFM)

2.1 AFM: What Is It?

Atomic force microscope (AFM) is an characterization instrument of nanoscience that is used to determine topography and other properties of surfaces [15, 16, 57, 73, 86]. The AFM can analyze the thick and thin films, metals, semiconductors, polymers, and composites. The Atomic Force Microscope (AFM) is also known as

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Chapter 3
Nanoelectronics Issues for Design for Excellence

1 Introduction

One nanometer is one-billionth of a meter or 10^{-9}. To comprehend how small is this dimension the width of human hair is approximately 80,000 nanometers (i.e.80 μm) [10]. In general, nanotechnology deals with matters and devices at the dimensions between less than 100 nanometers. The nanotechnolgy study encompasses nanoscale science, engineering, and technology. It involves design, imaging, measuring, modeling, manipulating, simulation, and characterization of nanoscale matters and devices as well as nanotechnology based circuits and system. Nanotechnology may be electrical or non-electrical in nature (e.g. nano-electro-mechanical systems NEMS). The nanoscale dimension electronics (called nanoelectronics) is the focus in this book. In nanoelectronics, devices, circuits and systems can be designed and fabricated. The nanoelectronic devices may include nanoscale CMOS or nano-CMOS field effect transistor (FET) (i.e. classical bulk CMOS FET), trigate FET, Graphene FET, Carbon Nanotune FET (CNTFET), etc. A selected key issues faced by nanoelectronics design engineers will be discussed in detail in this chapter. To give a strong understanding of design issues and challenges in nanoelectronics based circuits and systems, in particular process variation, this chapter includes discussions on the various devices. In addition fabrication processes are also presented.

2 Design for eXcellence (DFX)

The technology scaling while facilitates the use of smaller devices it allows to pack more number of those small devices in the same die area. Thus effectively reduces the cost of computation. The following are the compelling reasons for the technology scaling [5, 207]:

1. The technology scaling increases packing density of the devices in a die (or chip). As the MOSFET size decreases more number of such devices can be packed in the same die area.
2. The current drive which is manifested by the transconductance (g_m) enhances due to technology scaling. This will be evident from the following discussion. In general transconductance is defined as follows for saturation region:
$$g_m = \left(\frac{\partial i_d}{\partial v_{gs}}\right) = \left(\frac{W}{L}\right)\mu\left(\frac{\varepsilon_{ox}}{T_{ox}}\right)(V_{gs} - V_{Th})\,. \tag{1}$$
From the above expression it evident that the current drive of the transistor can increase by the following ways: (1) reducing the gate length, (2) reducing the oxide thickness, (3) increasing dielectric constant (by using high-κ dielectrics), and (4) decreasing the threshold voltage.
3. The technology scaling has reduced power dissipation per computation. This is simply can be explained by the fact that smaller devices are being switched to perform operations and operating voltage has been reduced with scaling.
4. The technology scaling results in smaller capacitances.
5. The technology scaling improves the frequency response.

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Chapter 4
Phase-Locked Loop (PLL) Component Circuits

1 Introduction

In this chapter a widely used analog/mixed-signal system, the phase-locked loop (PLL) is presented. Different types of PLLs will be introduced and the various typical components of the PLL system will be discussed in detail in this chapter. Earliest discussions of the PLL are dates back to 1923 [55]. PLLs got major attention in 1970 and eventually integrated circuits for PLLs were realized. The PLLs are omnipresent in the day to day circuits and systems. PLLs have diverse application is various digital, analog, and mixed-signal circuits and systems. For example, frequency synthesis, frequency demodulation, synchronization, tracking, and television sweep circuits are few diverse applications [34]. Different applications of PLL is categorized in Fig. 1. With the heavy usage of smart devices with high speed wireless communication facilities, the performance of PLLs is becoming increasing important for the overall system performance [33].

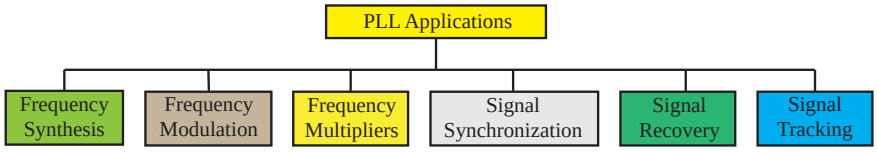

Fig. 1 Diverse Applications of Phase-Locked Loops (PLLs).

A simple usage of the PLL in the synchronous circuits and systems is depicted in Fig. 2. In these systems, there is a global clock signal which is understood and followed by all portions of the synchronous circuits and systems. Sequential elements like flip-flops, latches, and registers need the clock signal. PLLs drive clock distribution of a synchronous circuits and systems. The clock signals are typically efficiently generated by a phase-locked loop (PLL) for any target frequency.

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Chapter 5
Electronic Signal Converter Circuits

1 Introduction

In general signals are symbols or values with some ordering [15]. A signal is a function that conveys information or transfers energy [63]. Everyone handles some of the electronic signals at every moment of life. The signals may either available naturally or synthesized. The signal concept is depicted in Fig. 1. Electronic signal may in the form of video, image, or audio used for entertainment as well as information exchange. Signals may be the power supply signal in the form of alternating current or direct current. They may be communication signals in mobile communications, Wi-Fi, or Bluetooth. They are of different types such visible, nonvisible, or sound. They are of different dimensions, 1-D audio, 2-D images, or 3-D video. The signals may have different periods or clock cycle time. They can be of various frequencies such as radio frequency and audio frequency. The signals may be of diverse shapes; e.g. square, saw, or sine. The electronic signals may be either analog or digital in nature as depicted in Fig. 2. Analog signals are continuous in both value and time [15]. The discrete-time signals have values only at certain time stamps, i.e. continuous in value and discrete in time. The discrete-amplitude signals have only discrete values, i.e. discrete in value and continuous in time. The digital signals have discrete values and in addition discrete time. Both analog and digital signal electronic signals are encountered and processed all the time. Digital and discrete signals are obtained by sampling analog signals.

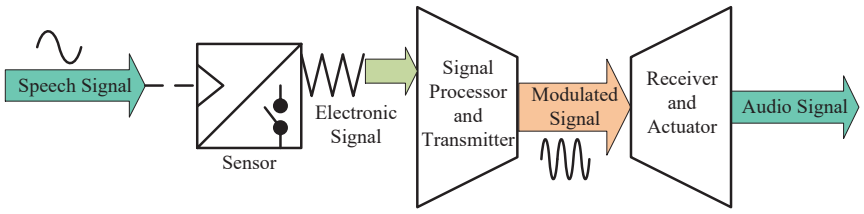

Fig. 1 Concept of a Typical Signal.

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Chapter 6
Sensor Circuits and Systems

1 Introduction

The energy appear in the universe in various forms including heat, mechanical, chemical (battery), and acoustics. The total energy of the universe is always constant as stated in the basic principles of energy conversion. However, the energy in various forms are always in continuous state of transformation or conversion from one form to other from. The broad term "transducers" covers all the devices needed for such energy conversion. Formally, the transducer is a device that converts one form of energy to another form of energy [93, 4, 3]. A list of showing selected different transducers is presented in Fig. 1.

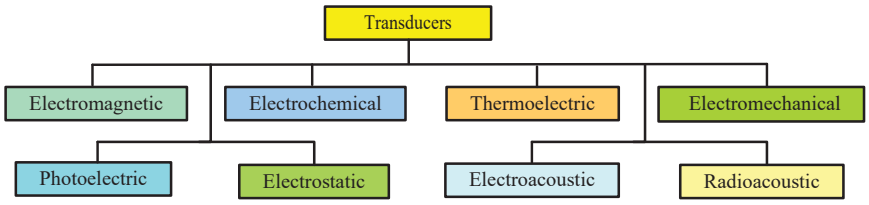

Fig. 1 Different Types of Transducers.

The transducers can measure and/or sense the following attributes such as light, temperature, force, speed, and sound [4, 3]. Simplistically, the transducers that convert nonelectrical energy to electrical energy are called "sensors". The transducers that convert electrical energy to mechanical energy are called "actuators". In this chapter the discussion will be limited to sensors i.e. transducers giving electronic signal as the output. Numerous types of sensor are designed and deployed in day-to-day applications as any physical parameters essentially can be sensed [43]. So, it is difficult to provide a comprehensive list. However, a selected types of different sensors are presented in Fig. 2.

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Chapter 7
Memory in the AMS-SoCs

1 Introduction

Memory is the key component of any computing platform. It performs its primary function of storing data, instructions, firmwires, system software, and application softwares. In addition it temporary stores data and instructions during the execution of an application or program. Depending on the usage of the memory, the memory can be of diverse types and forms. A selected types of memory types is presented in Fig. 1 [76]. The objective of any computing platform design is provide a large amount of memory to the users or programmers with a minimal cost. The cost, speed, and power dissipation of memory has affected the growth of VLSI technology and consumer electronics.

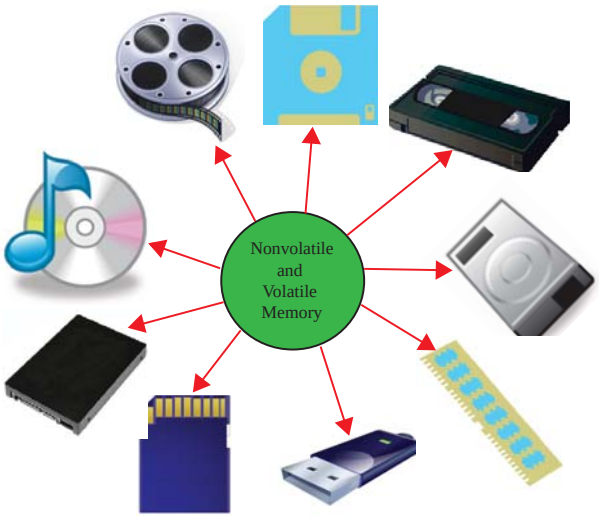

Fig. 1 Different Types of Memory in Various Computing Systems.

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Chapter 8
Mixed-Signal Circuit and System Design Flow

1 Introduction

A typical Analog/Mixed-Signal System-on-a-Chip (AMS-SoC) has a variety of components including digital processors, analog circuitry, RF circuitry, true mixed-signal circuitry integrated together to achieve cost and performance trade-offs [118, 67, 90, 62]. In addition there is significant software presence in the AMS-SoC in the form of firmware, system software (operating system), and application software. The design of power supply components which are battery packs and possibly accompanied by solar panel involves different design cycles. This chapter will focus on the hardware components involving analog, radio frequency (RF), digital, and mixed-signal circuitry.

In the hardware components of the AMS-SoC, the digital circuitry performs most of the back-end processing of the data. The mixed-signal, analog, and RF components are present for front-end processing including communications and interfacing. In a typical design style the digital components contain much more number of transistors as compared to the mixed-signal, analog, and RF components. Of course, the digital designs of well-defined abstraction like from system to physical level to provide design flexibility to design engineers through divide-and-conquer approach. However, at the last phase of the AMS-SoC design, all types of components (digital, mixed-signal, analog, and RF) are physical designs or layouts. At the circuit and the layout levels the designs go through analog SPICE simulations for verification and characterization. The complexity of the AMS-SoC hardware component designs have increased multifolds for many reasons including the following [90]:

(1) Integration of digital, analog, and mixed-signal functions along with the embedded software needs co-design for overall AMS-SoC optimization.
(2) New signal processing algorithms and their corresponding architectures provide much serious challenges in terms of total AMS-SoC power dissipation and performance requirements.
(3) The transistor count has increased tremendously to support the various functionalities of the AMS-SoC.
(4) The rapid change of the process technologies demands consideration of different technology parameters during the design cycle for simulation and design space exploration.

As a result the AMS-SoC design cycle is long and error prone. The overall design needs diverse skills, such as analog design, digital design, layout engineering, and design verification. The digital verification is becoming increasing important and complex. The need for analog verification has also emerged [64]. To make the situation worse the technically expected for such highly complex AMS-SoCs, the time-to-market has been reduced significantly. In such a situation, Computer Aided Design (CAD) environments including design and verification flows are more important than ever in order to produce error-free, affordable, and functional AMS-SoCs on time.

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Chapter 9
Mixed-Signal Circuit and System Simulation

1 Introduction

Breadboarding that involve prototyping of system using a breadboard with connector holes is not a feasible option for integrated circuit. The current generation equivalent of breadboarding for integrating circuits is simulation [248]. The simulation of the integrated circuits can help the overall design process during initial design phase, debugging phase, as well as during the diagnostic phase [176]. The simulation of integrated circuits or systems is the solving of the desired signals using computers [218]. In a general scale it may involve simulation for many aspects including the current signals, the voltage signals, the timing information, as well as power dissipation information. The simple concept of circuit and/or system is depicted in Fig. 1. The complete integrated circuit or overall system is made of the many different components or elements. The models of these components or elements are constructed in various different forms including mathematical expression, look-up-table (LUT), or plots that a computer can understand. The circuit or systems as well as the models are described in various languages that computer can understand with various simulation frameworks. The simulation engine that uses the models and circuit/system descriptions solves the circuit/system for specific input and setup conditions. The results obtained from the simulation are viewed as plain text data and/or graphical waveform viewers. This Chapter will discuss the simulation engines, various forms of circuit/system descriptions, and models in great details.

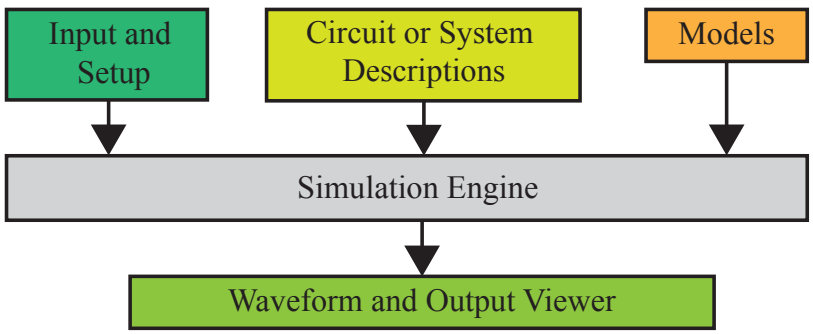

Fig. 1 The Concept of Integrated Circuit Simulation.

Simulation is every much essential as it provides insight of a circuit and/or system before it is being actually built [189, 278, 218]. The various possible forms of the simulations ensure that the circuit or system design is analyzed, characterized, and verified before proceeding to the next step in the design cycle. Hence stopping any propagation of design errors to next level of the design abstraction which may be difficult or costly to correct at a later stage. Thus, the design cycle time reduces, non-recurrent engineering (NRE) cost reduces, and the overall chip cost reduces. Simulations in the many different forms including ultra-fast system-level simulations, fast switch-level simulations, or slow SPICE simulations are used in various phases of the design flow for verification as well as characterization purposes. Fast and accurate simulations are needed for AMS-

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Chapter 10
Power, Parasitic, and Thermal Aware AMS-SoC Design Methodologies

1 Introduction

In a previous Chapter on Design for Excellence (DfX) a large set of issues which are encountered during the design of nanoelectronic based circuits and systems has been presented. Addresses one or more than one of these issues are challenging and they demand more efforts from system designer, design engineers, and layout engineers. The scope of this Chapter is the detailed discussion of a selected subset from DfX which was discussed in a previous Chapter. In particular, power, parasitics, and thermal issues have been discussed. In the case of power, static as well dynamic power dissipation have been presented along with their effects and techniques to handle them at various levels of design abstraction. The parasitics like resistors, capacitors, and inductors which arise from the active devices as well as passive interconnects can be origin of many problems such as performance and power dissipation. The parasitics can be distributed and lumped; the distributed are much more difficult to handle. The parasitics origin, modeling, and methods to handle during design flow have been presented in this Chapter. Then comes the thermal or temperature issue of the circuits and systems. The thermal issues are due to high on-chip heating due to high power dissipation or may be high ambient temperature. The on-chip thermal issues may arise from the high power dissipation. While the power dissipation issue and thermal issues have some commonalities they are different issues and may been different approaches to solve them. Therefore, this Chapter discusses the thermal issues as a different issue from power dissipation.

2 Power Dissipation: Remains Key Design Constraint

The research in low-power VLSI design has been one of the primary focus for last several decade [119, 175, 162, 40, 55, 32, 198, 27]. However, it still remains one of the major issues along with the additional emerging issues in the nanoelectronics era. The explosive growth of portable systems with serious computing capabilities have been a major driving factor of the low-power design. No doubt, with technology scaling and smaller feature size the devices are operated at low supply voltages. Hence it can be said the power dissipation of individual transistors per technology generation reduced. However, the number of transistors which are packed in the same die i.e. integration density of packing density of the chips increased have increased. It is estimated that with each generation, feature size has scaled by 0.7, integration density has increased by $2\times$, cost of computing reduced by $2\times$, while die size has minor increase of 14%. Thus the power consumption of the main stream chip have increased. In the recent years to operate with limited battery life, low-power system-on-a-chip (SoC) instead of pure hardware main stream microprocessors have been of quite demand. Of course, the in process the performance has been compromised. One can think why not having high performance battery a solution! First of all the chemical technology that is used in battery has its own limitations. The size of battery needed to provide higher current will not be helpful to make portable small electronic systems. In general the need for high-performance and yet portable small electronic systems and many other factors which are to be discussed in this Section have kept the power dissipation (including leakage dissipation) as the key constraint for the design engineers.

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Chapter 11
Variability-Aware AMS-SoC Design Methodologies

1 Introduction

Process variation has been discussed as a major issue in the Chapter on Design issues for DfX. Simplistically speaking process variations lead to discrepancy between sizes intended during the design time versus the sizes obtained during the manufacturing. For example, it is estimated that the variations in the channel length and threshold voltage of a MOSFET is as high as 30% in the case of a 65 nm CMOS process technology node [25, 28, 60]. The variations can be larger for further smalled process technology nodes. As depicted in Fig. 1(a), no two chips on the same wafer have same characteristics or even no two transistors in the same die are the same [50, 49, 4, 48, 11]. However, in a bigger perspective, the nanoelectronic parametric variations include, process variations (P), voltage variations (V), thermal variations (T), and transistor aging that takes place in nanoelectronic integrated circuits and systems [12, 20, 13, 64]. As presented in Fig. 1(b), the parameter variation can be either static or dynamic variations [12, 13]. The static parameter variations are caused by the variability in the manufacturing process; on the other hand, the dynamic parameter variations occurs in time during the operation of the circuit and system due to the changes in the environmental and workload conditions. The process variations originate from many possible sources as presented in Fig. 1(b) [50, 23]. As a result, the nature of process variations is quite different which can be at wafer level, at reticle level, and at local level. For the purpose of modeling and accurate statistical analysis they can be classifies in various ways as depicted in the figure. Many of these have been discussed in the Chapter on Design issues for DfX.

The process variations have significant negative impact on the integrated circuits, system-on-chips (SoCs) as well as multiple core systems in terms of their energy dissipation as well as performance characteristics [50, 49, 12, 20, 4, 48, 11, 64]. For example, the process variations affect functionality of design. The variations in the channel length can affects current carrying capability and delay. The variations in the threshold voltage can affects subthreshold leakage and delay. The process variations may change the characteristics of the circuits and system as compared to the design specification and hence may affect the yield. For example, not meeting the power dissipation or performance specifications even if the chip is fully functional is loss of yield in this competitive market. The design cycle is complicated and design engineers skills are really tested due to the process variations. For example, the number of process variation sources leads to more corner cases needed for meaningful simulations of the designs. The design decisions may need to be made based on statistical distributions rather than the actual characteristic data. Moreover, all these directly or indirectly affect the cost of the designed and fabricated circuits and systems. The cost may increase due to the increase in the design cost as well as due the reduction in the number of good chip resulted from the fabrications.

Variability tolerant design are necessary to produce robust circuits and systems with maximum possible yield and reduced cost. The important aspect is to incorporate variability awareness during the early stages of the design cycles such that the resulting chip is process variation tolerant. Such design flows for integrated circuits are called “process-variation tolerant” or “process-variation aware” design flows. For a quick reference such flows have been presented in Fig. 2 for both analog and digital integrated circuits [50, 49, 25, 28, 48]. The manufacturing process variations information for a specific manufacturing process needs be available to th design engineers for use at different levels of design abstractions. For example, what kind of variation channel lenght follow? For the integrated circuits, variability-aware analysis as well as variability-aware design optimization can be used. The variability-aware analysis techniques are needed for process-variation aware

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Chapter 12
Metamodel-Based Fast AMS-SoC Design Methodologies

1 Introduction

The design of various components of analog/mixed-signal system-on-a-chip (AMS-SoC) is quite complex and time intensive, specifically at the optimization and physical design stages [49, 83, 16, 23, 14, 59]. The parasitics present in the physical designs of AMS-SoC components which influence the circuits characteristics have significant impact on the numerical simulations. In order to reduce the design effort, design cycle, non-recurrent (NRE) cost, and overall the chip cost, fast and accurate AMS-SoC design optimization flow are needed. The design engineers can resort to various alternatives including the following: (1) Reduction of complexity of models (e.g. fast SPICE models, look-up tables) used in the circuit simulations. (2) Reduction of the simulation time by using fast numerical solvers. (3) Reduction of the design optimization time. (4) Reduction of the number of layout steps. The fast SPICE models, look-up tables (LUTs), reduced order models, macromodels, etc. speed up the simulation process. Macromodels are widely used in circuit simulations and verifications in the framework of EDA tools. Fast numerical solvers such as parallel solvers can speed up the simulation and design exploration as discussed in the Chapter on Mixed-Signal Circuit and System Simulation. Use of algorithms which can iterate faster and converge faster is always useful for speeding up the design process. The reduction of manual layout steps which are particularly used for mixed-signal and analog components and time consuming can speedup the design effort. Metamodel or surrogate (which is essentially model of a model i.e. mathematical model of a SPICE model) are used to perform design exploration either outside the EDA tools or high-levels of abstractions in the EDA tools to significantly speed up the design exploration of AMS-SoC components. This Chapter discusses a selected metamodel, metamodeling techniques, metamodel assisted analysis techniques, and metamodel assisted design flows.

2 Metamodels: An Overview

In this Section, various aspects of metamodel has been presented. The concept of metamodel has been introduced. The various different types of metamodels are briefly discussed. The important features of metamodels for accurate and efficient representation of the circuits or systems are discussed. Various technique used for error or accuracy analysis of metamodels is also presented.

2.1 Metamodel: Concept

A high-level idea of metamodel and metamodeling is depicted in Fig. 1 [45, 18, 80, 90, 32, 69, 68]. The schematic or layout of an integrated circuit is represented as a SPICE netlist or SPICE model. The SPICE netlist/model of the integrated circuit can be simulated and design exploration can be performed on it using an analog simulator or SPICE. This can be time consuming and computational intensive depending on the size and complexity of the integrated circuit. The SPICE netlist when simulated at the sample points of de-

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