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Models, Methods, and Tools for Complex Chip Design:

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Contents

Chapter 1
Polynomial Metamodel-Based Fast Optimization of Nanoscale PLL Components

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Abstract As the complexity of nanoscale-CMOS analog/mixed-signal (AMS) circuits and systems grows, the challenges of their design becomes exponentially more difficult. Performing accurate design simulations that entail exhaustive design space exploration has become infeasible with the increasing complexity of nano-CMOS circuits and systems integration, coupled with aggressive scaling of process technologies. Transistor-level SPICE simulations with full parasitics (RCLK) of complex circuits, which provide silicon accurate results, have run times in the order of days or weeks. With ever shrinking time to market pressures, the simulation time proves to be impractical as it can lead to longer design cycle times. The simulation time factor is further aggravated by additional design and process parameters which have to be accounted for due to increased sensitivity in deeply scaled technologies. In order to mitigate this problem, this chapter presents a two-stage approach that uses layout-accurate metamodels and efficient search algorithms for fast mixed-signal circuit and system optimization. The different components of a Phase-Locked Loop (PLL) are considered as a case study. First, the metamodel creation process is presented. A simulated annealing based optimization algorithm is then discussed for power optimization of the PLL components. It is shown that the metamodel approach speeds up the optimization phase by 2000$\times$ with very good accuracy. The power consumption of the circuit is decreased by 22% for the baseline design and is within 8% of the circuit netlist-based, but computationally expensive approach.

Key words: Analog/Mixed-Signal (AMS) Systems, AMS Circuits, Metamodels, Polynomial Metamodels, Phase-Locked Loop (PLL), Design Optimization

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