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Robust SRAM Designs and Analysis

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Robust SRAM Designs and Analysis

This book provides a guide to Static Random Access Memory (SRAM) bitcell design and analysis to meet the nano-regime challenges for CMOS devices and emerging devices, such as Tunnel FETs. Since process variability is an ongoing challenge in large memory arrays, this book highlights the most popular SRAM bitcell topologies (benchmark circuits) that mitigate variability, along with exhaustive analysis. Experimental simulation setups are also included, which cover nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis. Emphasis is placed throughout the book on the various trade-offs for achieving a best SRAM bitcell design.

- Provides a complete and concise introduction to SRAM bitcell design and analysis;
- Offers techniques to face nano-regime challenges such as process variation, leakage and NBTI for SRAM design and analysis;
- Includes simulation set-ups for extracting different design metrics for CMOS technology and emerging devices;
- Emphasizes different trade-offs for achieving the best possible SRAM bitcell design.

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