LECTURE NOTES IN ELECTRICAL ENGINEERING 58

Chao Huang
Editor

Robust Computing with Nano-scale Devices

Progresses and Challenges

Springer

Fault Tolerant Nano-Computing

Bharat Joshi[‡], Dhiraj K. Pradhan[†], and Saraju P. Mohanty[*]

[‡]*University of North Carolina-Charlotte, USA*

[†]*University of Bristol, UK*

[*]*University of North Texas, USA*

2.1 Introduction.

2.2 Principles of Fault Tolerant Nano-Computer Systems.

2.3 Process Variations in Nano-Scale Circuits.

2.4 Fault Tolerant Nano-Computer Applications.

2.5 Trends and Future.

Fault Tolerant Nanocomputing

Bharat Joshi, Dhiraj K. Pradhan, and Saraju P. Mohanty

Abstract This chapter provides an overview of fault tolerant nanocomputing. In general, fault tolerant computing can be defined as the process by which a computing system continues to perform its specified tasks correctly in presence of faults with the goal of improving the dependability of the system. Principles of fault tolerant nanocomputing as well as applications of the fault tolerant nanocomputers are discussed. The chapter concludes by observing trends in the fault tolerant nanocomputing.

Keywords Availability · Coverage · Dependability · Fault tolerance · Redundancy Reliability

Introduction

Fault tolerant computing can be defined as the process by which a computing system continues to perform its specified tasks correctly in presence of faults. These faults could be transient, permanent, or intermittent faults. A fault is said to be transient if it occurs for a very short duration of time. While permanent faults are the faults that continue to exist in the system, intermittent faults repeatedly appear for a period of time. They could be either hardware or software faults caused by errors in specification, design, or implementation, or faults caused by manufacturing defects. They could also be caused by external disturbances or simply due to ageing of the components in a system.

B. Joshi (✉)
University of North Carolina-Charlotte, USA
e-mail: bsjoshi@uncc.edu

D.K. Pradhan
University of Bristol, UK
e-mail: pradhan@compsci.bristol.ac.uk

S.P. Mohanty
University of North Texas, USA
e-mail: saraju.mohanty@unt.edu

C. Huang (ed.), *Robust Computing with Nano-scale Devices: Progresses and Challenges*, Lecture Notes in Electrical Engineering 58,
DOI 10.1007/978-90-481-8540-5_2, © Springer Science+Business Media B.V. 2010

A good viable alternative approach for fault tolerance would be to mimic biological systems. There is some activity in this area, but it is still in its infancy. For example, an approach to design complex computing systems with inherent fault tolerance capabilities based on the embryonics was recently proposed. Similarly, a fault detection, location, and reconfiguration strategy was proposed last year based on cell signaling, membrane trafficking, and cytokinesis [10].

Furthermore, the existing external infrastructure, such as Automatic Test Equipment (ATE), are not capable of dealing with the new defect levels that nanometer scale technologies create in terms of fault diagnosis, test time, and handling the amount of test data generated. In addition, continual development of ATE facilities that can deal with the new manufacture issues is not realistic. This has considerably slowed down the design of various system-on-a-chip efforts [62]. For example, while the embedded memory typically occupies half of the integrated circuits area their defect densities tend to be twice that of logic. Thus, to achieve and maintain cost advantages requires improving memory yields. As described earlier, one commonly used strategy to increase yield is to incorporate redundant elements that can replace the faulty elements during repair phase. The exiting external infrastructure cannot perform these tasks in a cost effective way. Thus, there is a critical need for on-chip (internal) infrastructure to resolve these issues effectively. The semiconductor industry has attempted to address this problem by introducing embedded intellectual property blocks called the infrastructure intellectual property (IPP). For embedded memory, the IPP may consist of various types of test and repair capabilities.

REFERENCES

1. Al-Yamani, A., Ramsundar, S., and Pradhan, D., “A Defect Tolerance Scheme for Nanotechnology Circuits,” *IEEE Transactions on Circuits and Systems*, vol. 54, no. 11, November 2007, pp. 2402-2409.
2. Bertoni, G., Breveglieri, L., Koren, I., Maistri, P., and Piuri, V., "Detecting and Locating Faults in VLSI Implementations of the Advanced Encryption Standard," in *Proc. of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* pp. 105-113, Nov. 2003.
3. Bhaduri, D. and Shukla, S., “NANOLAB – A tool for evaluating reliability of defect-tolerant nanoarchitectures,” *IEEE Transactions on Nanotechnology*, vol. 4, no. 4, July 2005, pp. 381-394.
4. Bhaduri, D., Shukla, S., Graham, P., and Gokhale, M., “Comparing reliability-redundancy tradeoffs for two von neuman multiplexing architectures,” *IEEE Transactions on Nanotechnology*, vol. 6, no. 3, May 2007, pp. 265-279.
5. Bowen N. and Pradhan, D., “Issues in Fault Tolerant Memory Management”, *IEEE Transactions on Computers*, August 1996, pp. 860-880.
6. Bowen, N., and Pradhan, D., "Processor and memory-based checkpoint and rollback recovery," *IEEE Computer*, Vol. 26, No. 2, Feb. 1993, pp. 22-31.
7. Chatterjee, M. and Pradhan D., “A GLFSR-Based Pattern Generator for Near-Perfect Fault Coverage in BIST”**,** *IEEE Transactions on Computers*, December 2003, pp. 1535-1542.
8. Chen, C., and Somani, A., "Fault Containment in Cache Memories for TMR Redundant Processor Systems," *IEEE Transactions on Computers*, Vol. 48, No. 4, March 1999, pp. 386-397.
9. Chillarege, R., and Iyer, R., “Measurement-Based Analysis of error latency,” *IEEE Transactions on Computers*, pp.529-537, May 1987.
10. Datta, K., Karanam, R., Mukherjee, A., Joshi, B., and Ravindran, A., “A Bio-Inspired Self-Repairable Distributed fault tolerant Design Methodology with Efficient Redundancy Insertion Technique,” in *Proceedings of the 16th IEEE NATW*, 2006.

11. DeHon, A., Goldstein, S., Kuekes, P. and Lincoln, P., “Nanophotolithographic nanoscale memory density prospects,” *IEEE Transactions on Nanotechnology*, vol. 4, no. 2, May 2005, pp. 215-228.
12. Drennan P. and McAndrew, C., “Understanding MOSFET mismatch for analog design,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, March 2003.
13. Elnozahy, E., Alvisi, L., Wang, Y., and Johnson, D., “A survey of rollback-recovery protocols in message-passing systems,” *ACM Computing Surveys*, vol. 34, no. 3, September 2002, pp. 375-408.
14. Gattiker, A., Haensch, W., Ji, B., Nassif, S., Nowak, E., Pearson, D., Bernstein, K., Frank, D., and Rohrer, N., “High-performance CMOS variability in the 65-nm regime and beyond,” *IBM Journal of Research and Development*, vol. 50, no. 4/5, pp. 433–449, July-September 2006.
15. Han, J and Jonker, P., “A system architecture solution for unreliable nanoelectronic devices,” *IEEE Transactions on Nanotechnology*, vol. 1, no. 4, December 2002, pp. 201-208.
16. Hayne, R. and Johnson, B., "Behavioral Fault Modeling in a VHDL Synthesis Environment", *Proceedings of the IEEE VLSI Test Symposium, Dana Point*, California, April 25-29, 1999, pp. 333-340.
17. Intel chips to shrink to 32-nanometer process, http://www.infoworld.com/article/07/09/18/Intel-chips-shrink-to-32-nanometer-process_1.html or http://www.intel.com/idf/.
18. Johnson, B., "Design and Analysis of Fault Tolerant Digital Systems," Addison-Wesley, 1989.
19. Joshi, B. and Hosseini, S. “Diagnosis Algorithms for Multiprocessor Systems,” in Proc. *IEEE Workshop on Embedded Fault-Tolerant Systems*, Boston, MA, 1998.
20. Kaufman, L., Bhide, S., and Johnson, B., "Modeling of Common-Mode Failures in Digital Embedded Systems", in *Proceedings of the IEEE Annual Reliability and Maintainability Symposium*, Los Angeles, California, January 24-27, 2000, pp. 350-357.
21. Koren, I. and Mani Krishna, C., “Fault-Tolerant Systems,” Morgan Kauffman Publishers, 2007.
22. Krishnaswamy, S., Markov, I., and Hayes, J., "Logic circuit testing for transient faults," in *Proceedings of the European Test Symposium* (ETS'05), 2005.
23. Lala, P., “Self-Checking and Fault Tolerant Digital Design,” Morgan Kaufmann, 2000.
24. Lamport, L., Shostak, S., and Pease, M., “The Byzantine Generals Problem,” *ACM Transactions of Programming Languages and System*, July 1982, pp. 382-401.
25. Li, M., Goldberg, D., Tao, W., and Tamir, Y., “Fault-Tolerant Cluster Management for Reliable High-Performance Computing,” in *Proc. of the 13th International Conference on Parallel and Distributed Computing and Systems*, Anaheim, CA, pp. 480-485 (August 2001).
26. Liu, C., and Pradhan, D., “EBIST: A Novel Test Generator with Built-In-Fault Detection Capability”, *IEEE Transactions on CAD,* Volume 24, No. 8, August 2005.
27. Lyu, M., editor, “Software Reliability Engineering,” McGraw Hill, 1996.
28. Maheshwari, A., Koren, I., and Burleson, W., “Techniques for Transient Fault Sensitivity Analysis and Reduction in VLSI Circuits,” *Defect and Fault Tolerance in VLSI Systems*, 2003.
29. Messer, A., Bernadat, P., Fu, G., Chen, D., Dimitrijevic, Z., Lie, D., Mannaru, D., Riska, A., and Milojicic, D., "Susceptibility of commodity systems and software to memory soft errors," *IEEE Transactions on Computers*, Vol. 53, No. 12, pp.1557-1568, Dec. 2004.
30. Mohanty, S. and Kougianos, E., "Simultaneous Power Fluctuation and Average Power Minimization during Nano-CMOS Behavioral Synthesis", in *Proceedings of the 20th IEEE International Conference on VLSI Design (VLSID)*, pp. 577-582, 2007.

31. Mohanty, S. and Kougianos, E., "Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates", in *Proceedings of the 24th IEEE International Conference on Computer Design (ICCD)*, pp. 210-215, 2006.
32. Mohanty, S., Kougianos, E., Ghai D., and Patra, P., "Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, pp. 207-213, 2007.
33. Mohanty, S., Ranganathan N., Kougianos, E., and Patra, P., Low-Power High-Level Synthesis for Nanoscale CMOS Circuits, 1st Edition, Springer, 2008.
34. Nikolic, K., Sadek, A. and Forshaw, M., “Fault-tolerant techniques for nanocomputers,” *Nanotechnology*, vol. 13, 2002, pp. 357-362.
35. Oh, N., Shirvani, P., and McCluskey, E., "Error detection by duplicated instructions in superscalar processors*,"* *IEEE Transactions on Reliability*, Vol. 51, pp. 63-75.
36. Omari, R., Somani, A., and Manimaran, G., "An adaptive scheme for fault-tolerant scheduling of soft real-time tasks in multiprocessor systems," *Journal of Parallel and Distributed Computing*, Vol. 65, no. 5, pp. 595-608, May 2005.
37. Papadopoulou, E., “Critical Area Computation for Missing material Defects in VLSI Circuits,” *IEEE Transactions on CAD*, vol. 20, pp. 503-528, May 2001.
38. Peper, F., Lee, J., Abo, F., Isokawa, T., Adachi, S., Matsui, N., and Mashiko, S., “Fault tolerance in nanocomputers: a cellular array approach,” *IEEE Transactions on Nanotechnology*, vol. 3, no. 1, March 2004, pp. 187-201.
39. Pradhan, D. (editor), "Fault-Tolerant Computer System Design," Prentice Hall, 1996.
40. Pradhan, D., and Vaidya N., “Roll-Forward Checkpointing Scheme: A Novel fault-Tolerant Architecture” *IEEE Transactions on Computers*, vol. 43, no. 10, October 1994, 1163-1174.
41. Qi, Y., Gao, J., and Fortes, J., “Markov chains and probabilistic computation – a general framework for multiplexed nanoelectronic systems,” *IEEE Transactions on Nanotechnology*, vol. 4, no. 2, March 2005, pp. 194-205.
42. Ramesh, A., Twigg, D. , Sandadi, U., Sharma, T., Trivedi, K., and Somani, A., “Integrated Reliability Modeling Environment," *Reliability Engineering and System Safety*, Elsevier Science Limited; UK, Volume 65, Issue 1, March 1999, pp. 65 - 75.
43. Reis, G., Chang, J., Vachharajani, N., Rangan, R., August, D., and Mukherjee, S., "Software-Controlled Fault Tolerance," *ACM Transactions on Architecture and Code Optimization*, pp.1-28, December 2005.
44. Roy, S, and Beiu, V., “Majority multiplexing – economical redundant fault-tolerant designs for nanoarchitectures,” *IEEE Transaction on Nanotechnology*, vol. 4, no. 4, July 2005, pp. 441-451.
45. Schmid, A. and Leblebici, Y., “A Highly Fault Tolerant PLA Architecture for Failure-Prone Nanometer CMOS and Novel Quantum Device Technologies,” *Defect and Fault Tolerance in VLSI Systems*, 2004
46. Schwab, A., Johnson, B., and Bechta-Dugan, J., "Analysis Techniques for Real-Time, Fault-Tolerant, VLSI Processing Arrays", in *Proceedings of the 1995 IEEE Annual Reliability and Maintainability Symposium*, Washington, DC, January 17-19, 1995, pp. 137-143.
47. Sharma, D. and Pradhan, D., “An Efficient Coordinated Checkpointing Scheme for Multicomputers,” Fault-Tolerant Parallel and Distributed Systems, IEEE Computer Society Press, 1995.
48. Shivakumar, P., Kistler, M., Keckler, S., Burger, D., and Alvisi, L., "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Proceedings of the 2002 International Conference on Dependable Systems and Networks*, 2002, pp. 389-399.
49. Shooman, M., “Reliability of Computer Systems and Networks,” Wiley Inter-Science, 2002.
50. Siewiorek, D. (editor), “Fault Tolerant Computing Highlights from 25 Years,” in *Special volume of the 25th International Symposium on Fault-Tolerant Computing FTCS-25*, Pasadena, CA.

51. Siewiorek, D. and Swartz, R., “The Theory and Practice of Reliable System Design,” A. K. Peters, 1999.
52. Singh, J., Mathew, J., Mohanty, S., and Pradhan, D., “Statistical Analysis of Steady State Leakage Currents in Nano-CMOS Devices”, in *Proceedings of the 25th IEEE Norchip Conference (NORCHIP)*, 2007.
53. Somani, A., and Vaidya, N., "Understanding fault tolerance and reliability," *IEEE Computer*, April 1997, pp. 45-50.
54. Strukov, D. and Likharev, K., “Defect-tolerant architectures for nanoelectronic crossbar memories,” *Journal of Nanoscience and Nanotechnology*, vol. 7, no. 1, January 2007.
55. Strukov, D. and Likharev, K., “Prospects for terabit-scale nanoelectronic memories,” *Nanotechnology*, vol. 16, January 2005, pp. 137-148.
56. Sun, F. and Zhang, T., “Defect and transient fault-tolerant system design for hybrid CMOS/nanodevice digital memories,” *IEEE Transactions on Nanotechnology*, vol. 6, no. 3, May 2007, pp. 341-351.
57. Tahoori, M., “Defects, Yield, and Design in Sublithographic Nano-Electronics,” *Proceedings of the 2005 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, 2005.
58. Vaidya, N. and Pradhan, D., “Fault-Tolerant Design Strategies for High Reliability and Safety,” *IEEE Transactions on Computers*, vol. 42, no. 10, October 1993.
59. von Neumann, J. “Probabilistic Logics and the Synthesis of Reliable Organisms from Unreliable Components,” *Automata Studies, Annals of Mathematical Studies*, Princeton University Press, No. 34, 1956, pp. 43-98.
60. Welke, S., Johnson, B., and Aylor, J., "Reliability Modeling of Hardware-Software Systems", *IEEE Transactions on Reliability*, Vol. 44, No. 3, September 1995, pp. 413-418.
61. Zhang, Y., and Chakrabarty, K., "Fault Recovery Based on Checkpointing for Hard Real-Time Embedded Systems," in *Proceedings of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems* (DFT'03), 2003.
62. Zorian, Y., and Chandramouli, M, “Manufacturability with Embedded Infrastructure IPs, http://www.evaluationengineering.com/archive/articles/0504/0504embedded_IP.asp.