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Low-Power High-Level Synthesis for Nanoscale CMOS Circuits

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Contents

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Low-Power High-Level Synthesis for Nanoscale CMOS Circuits

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis, characterization, estimation, and optimization of the various forms of power dissipation in the presence of process variations of nano-CMOS technologies. The authors show very large-scale integration (VLSI) researchers and engineers how to minimize the different types of power consumption of digital circuits. The material deals primarily with high-level (architectural or behavioral) energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate/transistor level. At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms, the power reduction opportunities are greater, and it can cost-effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation.

The book is a self-contained low-power, high-level synthesis text for Nanoscale VLSI design engineers and researchers. Each chapter has simple relevant examples for a better grasp of the principles presented. Several algorithms are given to provide a better understanding of the underlying concepts. The initial chapters deal with the basics of high-level synthesis, power dissipation mechanisms, and power estimation. In subsequent parts of the text, a detailed discussion of methodologies for the reduction of different types of power is presented including:

- Power Reduction Fundamentals
- Energy or Average Power Reduction
- Peak Power Reduction
- Transient Power Reduction
- Leakage Power Reduction

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low-power CMOS circuits.

ISBN 978-0-387-76473-3

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